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Radiation-Hard ASICs for Optical Data Transmission in the ATLAS Pixel Detector

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We have developed two radiation-hard ASICs for optical data transmission in the ATLAS pixel detector at the CERN Large Hadron Collider (LHC): a driver chip for a Vertical Cavity Surface Emitting Laser (VCSEL) diode for 80 Mbit/s data transmission from the detector, and a Bi-Phase Mark decoder chip to recover the control data and 40 MHz clock which is received optically by a PIN diode on the detector side. We present comprehensive results from the final design and from irradiation studies of both circuits with 24 GeV protons up to a total dose of 62 Mrad.

1. Introduction

The ATLAS pixel detector [1] consists of two barrel layers, two forward, and two backward disks which provide at least two space point measurements. The pixel sensors are read out by front-end electronics controlled by the Module Control Chip (MCC). The low voltage differential signal (LVDS) from the MCC is converted by the VCSEL Driver Chip (VDC) into a single-ended signal appropriate to drive a VCSEL. The optical signal from the VCSEL is transmitted to the Readout Device (ROD) via a fiber.

The 40 MHz beam crossing clock from the ROD, bi-phase mark (BPM) encoded with the data (command) signal to control the pixel detector, is transmitted via a fiber to a PIN diode. This BPM encoded signal is decoded using a Digital Opto-Receiver Integrated Circuit (DORIC). The clock and data signals recovered by the DORIC are in LVDS form for interfacing with the MCC.

The ATLAS pixel optical link system contains 448 VDCs and 360 DORICs with each chip containing four channels. The chips couple to 224 VCSEL and 180 PIN array optical packages (opto-packs). The chips and optopacks are mounted on 180 chip carrier boards (opto-boards). The pixel optical link circuitry is expected to be exposed to 10^{15} 1-MeV n_{eq}/cm^2 during ten years of operation at the LHC. We present results from the final design and from irradiation studies of both circuits with 24 GeV protons up to a total dose of 62 Mrad.

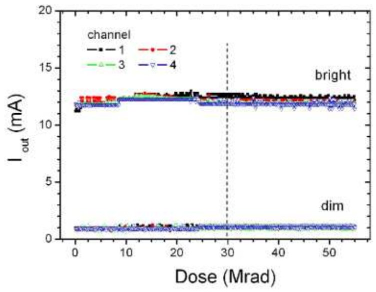

Fig. 1. Bright and dim output current for four VDC channels versus radiation dosage. The dashed line shows the expected VDC lifetime dose at LHC.

2. Circuit Description

The VDC and DORIC have been implemented in the standard deep submicron (0.25 μm) CMOS technology, which has a nominal supply voltage of 2.5 V. By employing enclosed layout transistors and guard rings [2], this technology has proven to be very radiation hard.

The VDC converts an LVDS input into a single-ended signal appropriate to drive a VCSEL. The output current is adjustable between 0–20 mA, with a standing dim current of 1 mA to improve the VCSEL switching speed. The rise and fall times of the output signal are nominally less than 1 ns for 80 Mbit/s signals. In order to reduce noise on the opto-board, the VDC must have constant current consumption.

The DORIC decodes BPM encoded clock and command signals received by a PIN. The amplitude of the current from the PIN diode is expected to be in the range of 40–1000 μA. The 40 MHz clock recovered by the DORIC is required to have a duty cycle of $(50 \pm 4)\%$ with a total timing error (jitter) less than 1ns. The bit error rate of the DORIC is required to be less than 10^{-11} at end of life.

3. Irradiation Studies

We have performed radiation-hardness studies of the VDC and DORIC circuits using 24 GeV protons at CERN in September 2003 up to a total dose of 62 Mrad. Four 4-channel VDC and DORIC chips were tested electrically with no optical components, allowing direct study of the possible degradation of the chips without the additional complications from the optical components. Irradiation studies of previous prototypes of these circuits revealed no degradation up to a dose of 57 Mrad.

The VDC is sent an LVDS signal and drives a 50Ω resistor instead of a VCSEL. The rise and fall times, output duty cycle, as well as the bright and dim output currents are monitored as a function of dosage. We observe no significant degradation in the rise and fall times or output duty cycle. Figure 1 likewise shows no degradation in the measured bright and dim currents versus dose.

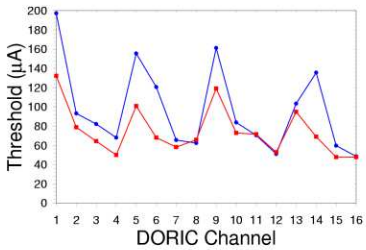

Fig. 2. Threshold for no bit errors before (circles) and after (squares) irradiation for 16 DORIC channels.

The DORIC is sent a variable signal with adjustable amplitude over a long coaxial cable instead of being driven optically by a PIN diode. The threshold current for no bit errors, as well as the recovered clock duty cycle and jitter are monitored versus dose. The threshold current for no bit errors [3] is unchanged after irradiation (Fig. 2). The clock duty cycle of one DORIC channel moved slightly out of spec after irradiation (45.5%; the spec is $(50 \pm 4)\%$). The jitter of the recovered clock is unchanged after irradiation.

4. Summary

The VDC and DORIC circuits implemented in the standard deep submicron (0.25 μm) technology meet all the requirements for operation in the ATLAS pixel detector's optical readout system. The circuits appear sufficiently radiation hard for ten years of operation at the LHC. Production of these chips is complete; the chips are an integral part in the production of opto-boards which will be installed in the ATLAS detector.

Acknowledgments

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References

1. ATLAS Pixel Detector Technical Design Report, CERN/LHCC/98-13.
2. G.Anelli *et al.*, IEEE Trans. on Nucl. Sci., Vol. 46 (1999) 1690.
3. The threshold current for no bit errors and the duty cycle of the recovered clock improve with shorter wirebonds and traces than those used during the irradiation studies; shorter wirebonds and traces will be implemented on the opto-board.