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DESIGN, PREPRODUCTION, AND PERFORMANCE OF THE CDF RUN IIB SILICON DETECTOR

PAUL LUJAN*
for the CDF Run IIb Silicon collaboration
Lawrence Berkeley National Laboratory, 1 Cyclotron Road
Berkeley, CA 94720, USA

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A new silicon detector was designed by the CDF collaboration for Run IIb of the Tevatron at Fermilab. The main building block of the new detector is a “supermodule” or “stave”, an innovative, compact and lightweight structure of several readout hybrids and sensors with a bus cable running directly underneath the sensors to carry power, data, and control signals to and from the hybrids. The hybrids use a new, radiation-hard readout chip, the SVX4 chip. A number of SVX4 chips, readout hybrids, sensors, and supermodules were produced and tested in preproduction. The performance (including radiation-hardness) and yield of these components met or exceeded all design goals. The detector design goals, solutions, and performance results are presented.

Keywords: CDF Run IIb; SVX4; stave; supermodule; silicon tracker

1. Introduction

The CDF Run IIb silicon detector was designed[1] as a replacement for the current silicon detector at CDF, as it was necessary to deal with the higher expected radiation levels during Run IIb of the Tevatron. The new detector features a new, radiation-hard readout chip, the SVX4, and an innovative “stave” or “supermodule” design which carries several readout hybrids and sensors in a single compact, integrated package. This paper presents the results of our preproduction and testing.

2. Design Goals and Motivations

Run IIb of Fermilab was expected to deliver a total luminosity of 15 fb^{-1}, while the current CDF silicon detector was only rated to survive 4-8 fb^{-1} in the innermost layers.[2] Hence, an upgrade was necessary to preserve CDF’s silicon tracking ability, which is of vital importance to many parts of the physics program. While a partial upgrade of only the innermost layers was considered, a complete upgrade of the entire inner silicon tracker (not including the intermediate silicon layers) was determined to be the only practical method due to its simplicity.

*pjlujan@lbl.gov

To provide increased radiation tolerance, a new, radiation-hard readout chip, the SVX4, was designed. The new layout also called for the use of single-sided radiation-hard sensors, instead of the double-sided sensors used previously. To minimize the total amount of material used in the detector, the new "supermodule" design was developed to produce a compact, efficient structure, helping to compensate for the use of single-sided sensors. The supermodule design also allows for uniform layout in almost all layers, greatly simplifying the overall design. The innermost layer (L0) required a slightly different design, with narrower sensors and smaller hybrids.[3]

3. Detector Components

The SVX4 chip[4] is a radiation-hard mixed-signal ASIC built using commercial 0.25 μm CMOS technology. It is similar to the previous chip, the SVX3D, but it uses "radiation-hard by design" layout principles to achieve radiation hardness while avoiding the need for a custom process, thus greatly reducing costs and increasing yield. Important features of the SVX4 include sparsification (the ability to read out only channels above a configurable threshold), real-time pedestal subtraction, and deadtimeless operation, a feature where the analog front-end part of the chip continues to acquire data while the digital back end is digitizing and reading out.

Extensive testing was performed to ensure that in deadtimeless operation, the operation of the back end would not affect the data acquired by the front end. The data showed excellent stability, with a variation of at most 1-2 ADC counts during various back-end operations. (A minimum-ionizing particle, or MIP, is expected to produce a signal of approximately 50 ADC counts.) The chip was also subjected to radiation testing, and showed no variation in its performance for radiation doses in excess of 20 MRad, as well as excellent tolerance against single-event upsets (SEUs).

The SVX4 chips were mounted onto 4-chip hybrids, made of a beryllia substrate with traces printed using a fine-pitch thick film technology.[5] The hybrid technology was very similar to that used previously, so the design was relatively straightforward.

The silicon sensors are single-sided p^+ doped strips on n-doped bulk silicon. They are able to withstand high particle fluences and are designed to operate at high bias voltages to ensure full depletion. Two types of sensors were produced, axial and small-angle (1.2°) stereo. The sensors were tested and showed excellent radiation tolerance and leakage current, and met all performance goals.[6]

4. Supermodules

One of the principal design innovations in the Run IIb design was the use of a "supermodule" design[7] (illustrated in Figure 1). A supermodule consists of a carbon-fiber core with embedded cooling tubes, with a bus cable to carry signals, power and high voltages to and from the hybrids glued on either side, followed by an aluminum shield. The sensors are mounted on top of the shield, with six readout hybrids mounted on top of the sensors. A mini-port card[8], which serves as a transceiver for signals to and from the supermodule, sits at the end of the supermodule.

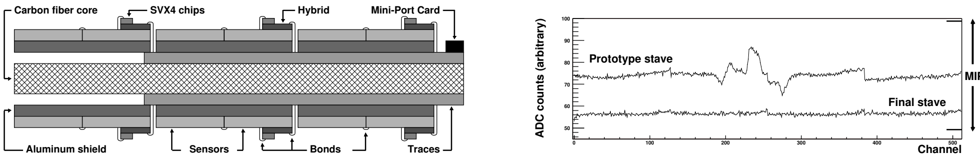

Fig. 1. Left: A schematic side view (not to scale) of a supermodule. Right: Sample pickup for all channels at an arbitrary moment in time during readout for a prototype supermodule (top line) and the final supermodule design (bottom line). The expected signal of a MIP is shown for comparison.

The main design challenge in the supermodule was ensuring that the close proximity of the bus cable to the silicon sensors did not result in pickup in the sensors of the signals in the bus cable. Early prototype supermodules exhibited considerable signal fluctuations during readout due to this pickup and other bus cable effects. However, improved bus cable layout and a thicker (50 μm) shield virtually eliminated all pickup problems.[9,10] Figure 1 shows the results.

5. Conclusion

The SVX Run IIb upgrade was canceled in September 2003 due to lowered luminosity projections for the Tevatron. However, we hope that the technologies developed will prove useful to later experiments. The SVX4 chip was a very successful design; it is being used in the DØ inner silicon layer upgrade, and several other experiments have expressed interest. Demonstrating the viability of the "supermodule" layout is also important, for example, for future silicon tracker upgrades at Super LHC.

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