Radiation-Hard ASICs for Optical Data Transmission in the ATLAS Pixel Detector

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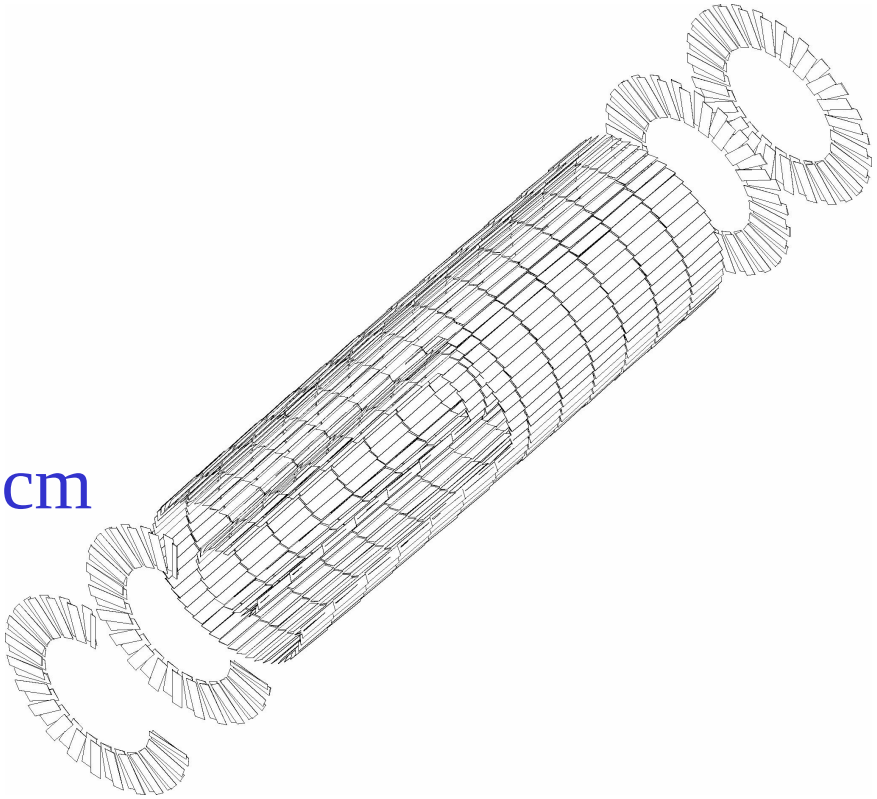
Outline

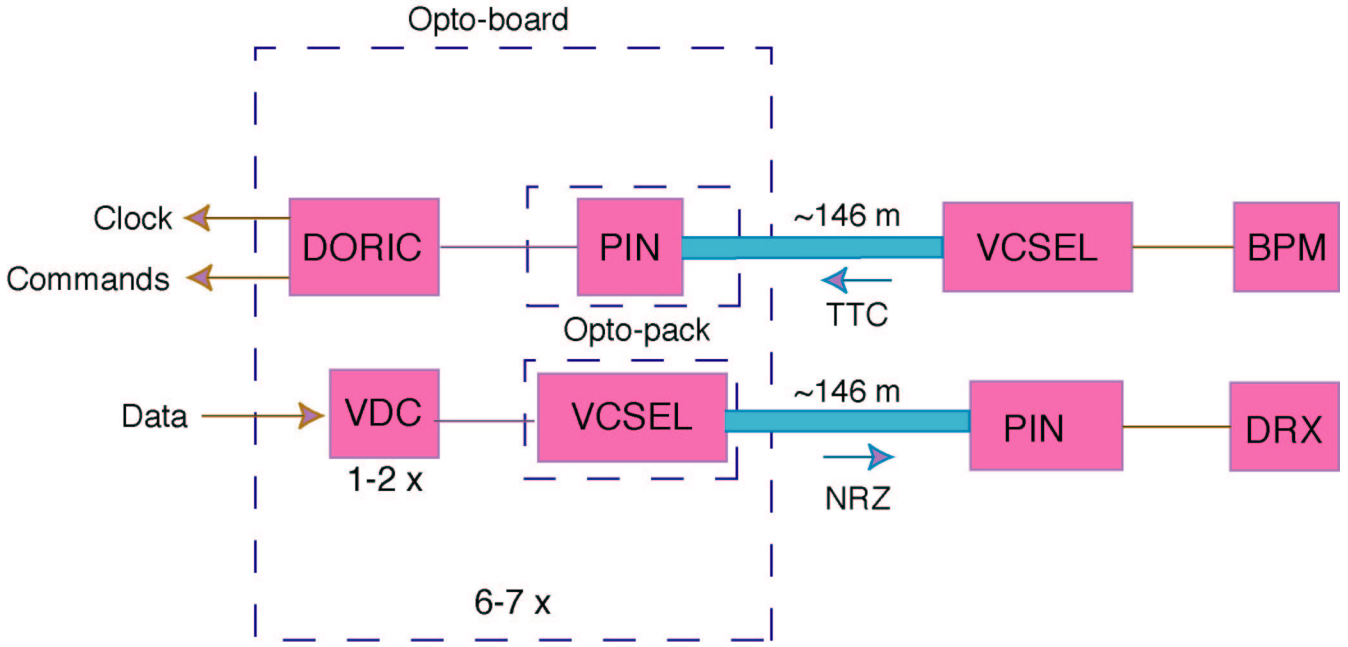
- Introduction
- ASIC description
- Proton irradiation
- Summary

ATLAS Pixel Detector

- Inner most tracking detector
- Pixel size: 50 μm x 400 μm
- 100 million channels
- Barrel layers at r = 5.1, 12.3 cm
- Disks at z = 50, 65 cm
- Dosage after 10 years:
  - optical link: 30 Mrad or 6 x 10^{14} 1-MeV n_{eq}/cm^2



ATLAS Pixel Opto-link



VCSEL: **Vertical Cavity Surface Emitting Laser diode**

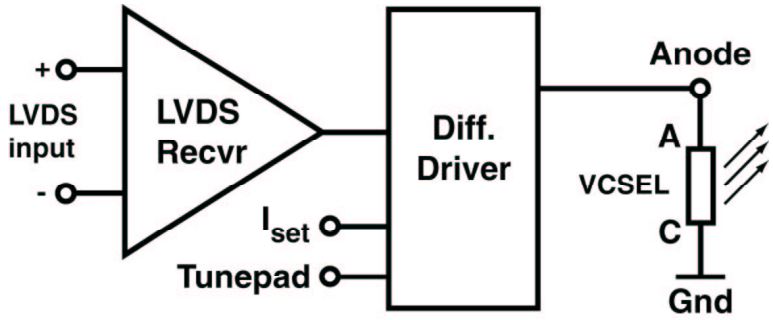
VDC: **VCSEL Driver Circuit**

PIN: **PiN diode**

DORIC: **Digital Optical Receiver Integrated Circuit**

VDC: VCSEL Driver Circuit

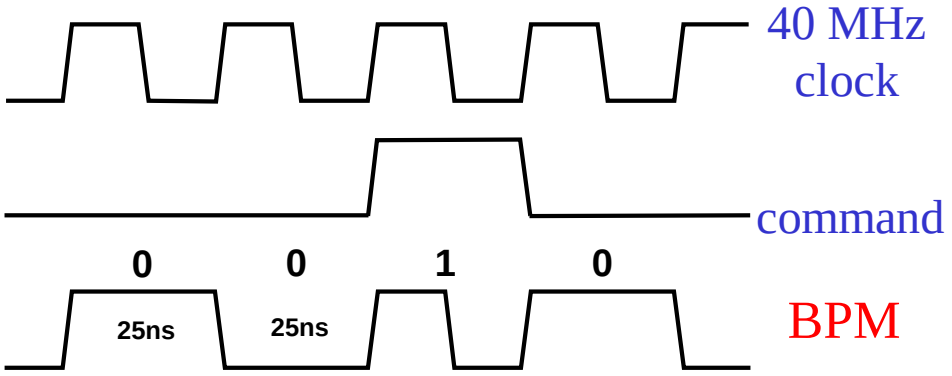
- Convert LVDS input signal into single-ended signal appropriate to drive VCSEL diode
- Output (bright) current: 0 to 20 mA
  - controlled by external current I_{set}
- Standing (dim) current: ~ 1 mA
  - improve switching speed

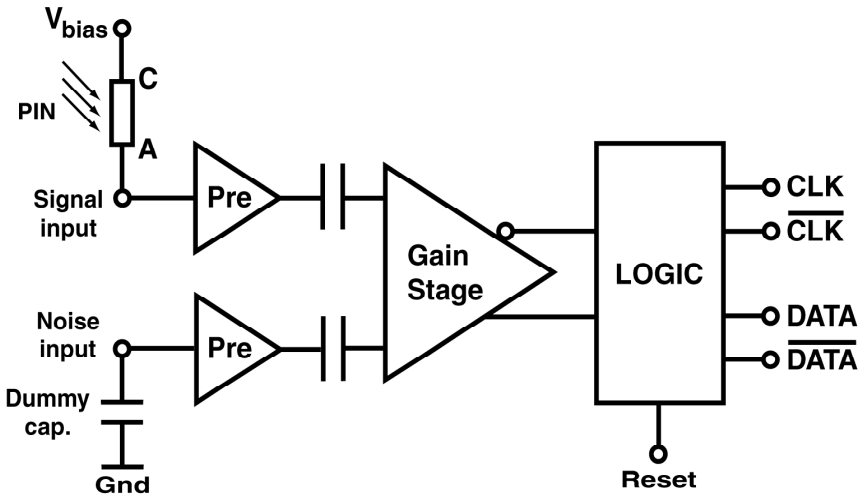


- Rise & fall times: 1 ns nominal for 80 MHz signals
- "On" voltage of VCSEL: up to 2.3 V at 20 mA for 2.5 V supply
- Constant current consumption!
- Use Truelight high-power oxide common cathode VCSEL array
- 512 4-channel chips needed for production

DORIC: Digital Optical Receiver IC

- Decode Bi-Phase Mark encoded (BPM) clock and command signals from PIN diode
- Input signal: 40-1000 μA
- Extract: 40 MHz clock
- Duty cycle: (50 ± 4)%
- Total timing error: < 1 ns
- Bit Error Rate (BER): $< 10^{-11}$ at end of life
- Use Truelight common cathode PIN array
- 424 4-channel chips needed for production



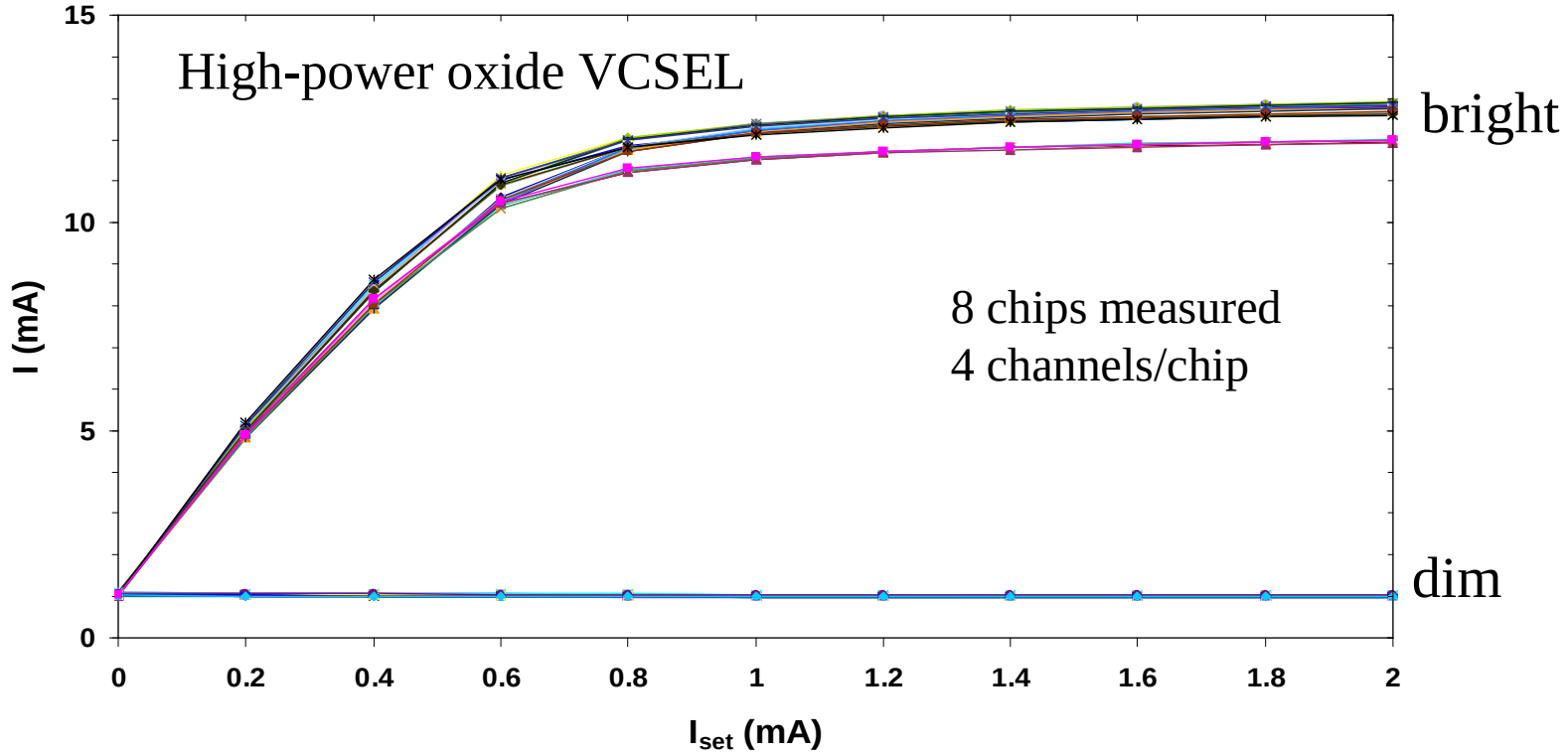


Status of VDC & DORIC

- Original design for ATLAS SemiConductor Tracker (SCT)
  - AMS 0.8 μm BiPolar in radiation tolerant process (4 V)
- DMILL #1-3: Summer 1999 - May 2001
  - 0.8 μm CMOS rad-hard process (3.2 V)
  - VDC & DORIC #3: meet specs
  - severe degradation of circuit performance in April 2001 proton irradiation
- IBM #1-5: Summer 2001 - Dec 2002
  - 0.25 μm CMOS rad-hard process (2.5 V)
  - enclosed layout transistors and guard rings for improved radiation hardness
- IBM 5e: April 2003 engineering run
  - convert 3-layer to 5-layer layout for submission with pixel Module Control Chip (MCC) for cost saving

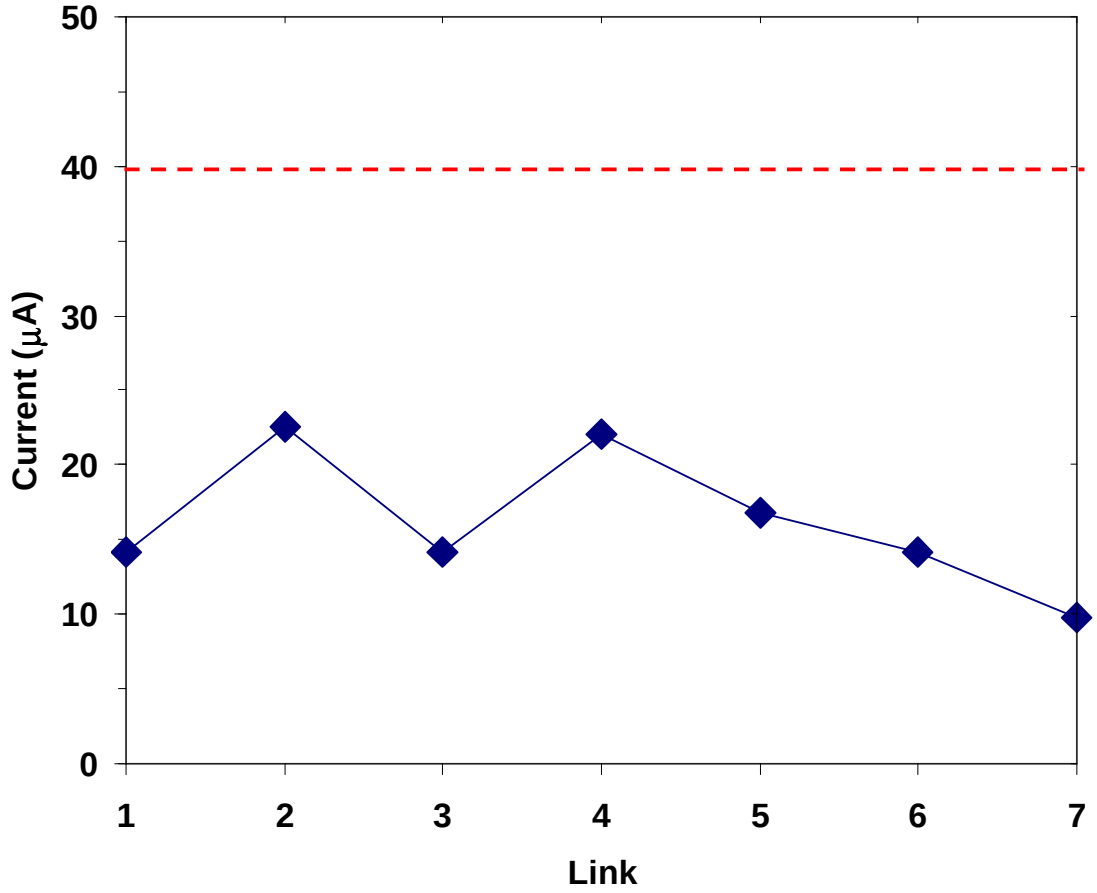
⇨ this is the production run since chips meet specs and sufficient quantity of chips were produced

VDC-I5e: Bright and Dim Currents vs. I_{set}



- dim current is ~ 1 mA as expected
- bright current measured with 1 Ω in series
- maximum bright current is ~ 13 mA
  - target is 20 mA but 13 mA is adequate for annealing from irradiation damage

DORIC: PIN Current Thresholds with No Bit Errors

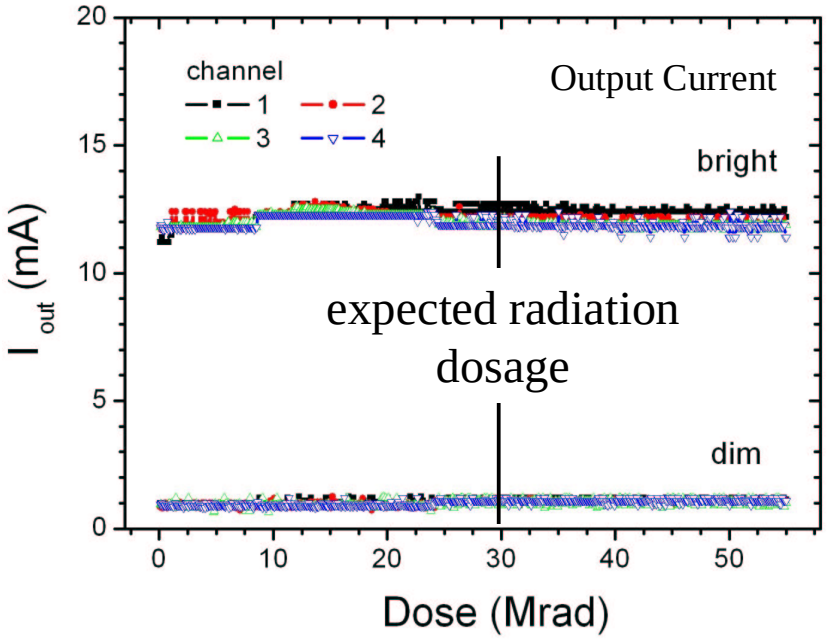


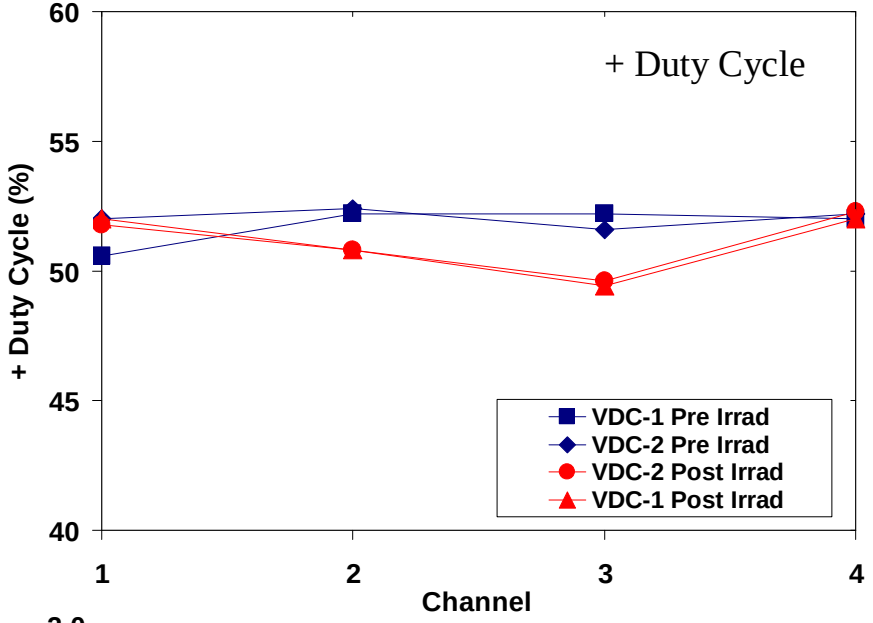
- thresholds significantly better than spec: 40 μA

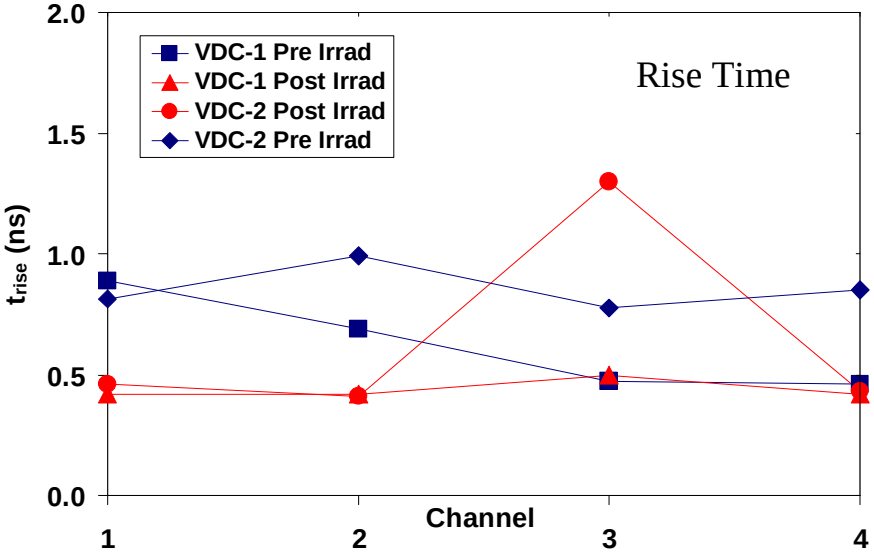
Proton Irradiation (Aug./Sept. 2003)

- production DORICs and VDCs irradiated with 24 GeV proton test-beam at CERN (T7) up to 62 Mrad
- VDC chips were driving 50 Ω load
  - measured “bright” and “dim” currents, output signal rise/fall times, duty cycle as a function of radiation dosage
  - ✓ no significant degradation was observed
- DORIC chips were sent a variable signal over a long coaxial cable
  - measured BER threshold, recovered clock duty cycle, jitter as a function of radiation dosage
  - ✓ no significant degradation was observed

VDC Performance

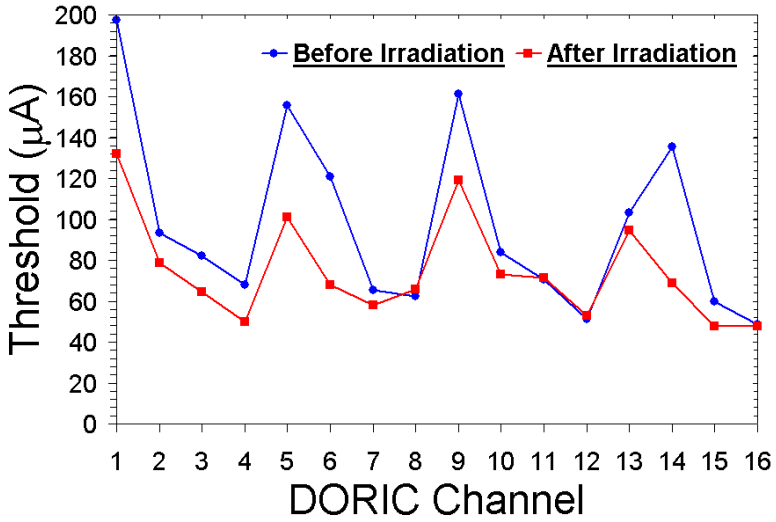


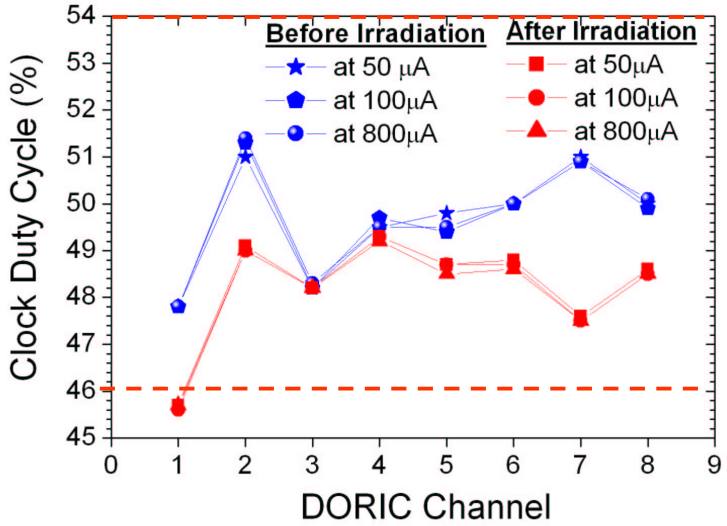




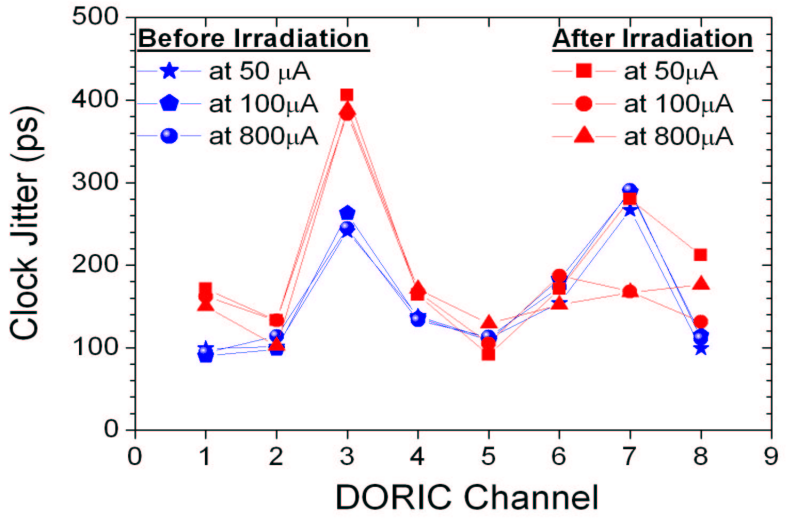
- ✓ Output current is constant vs. dose
- ✓ Duty cycle, rise/fall times consistent before and after irradiation
- ● measured rise/fall times better with shorter wirebonds and traces

DORIC Performance





- ✓ BER threshold unchanged after irradiation
- ✓ Clock duty cycle *slightly* out of spec after irradiation
  - Min 45.5% (spec 50±4%)
- ✓ Jitter consistent before and after irradiation (< 1ns)
- Threshold and duty cycle improve with shorter wirebonds and traces



Summary

- VDC-I5e & DORIC-I5e produced in IBM 0.25 μm
- radiation hard up to 62 Mrad
- meet or exceed ATLAS pixel specs
- production is completed

- Next Step: use VDC and DORIC on optical hybrid board
  ⇨ see Amir Rahimi's presentation (next)