Upgrade of the D0 Detector: The Tevatron Beyond 2fb^{-1}

Breese Quinn, University of Mississippi

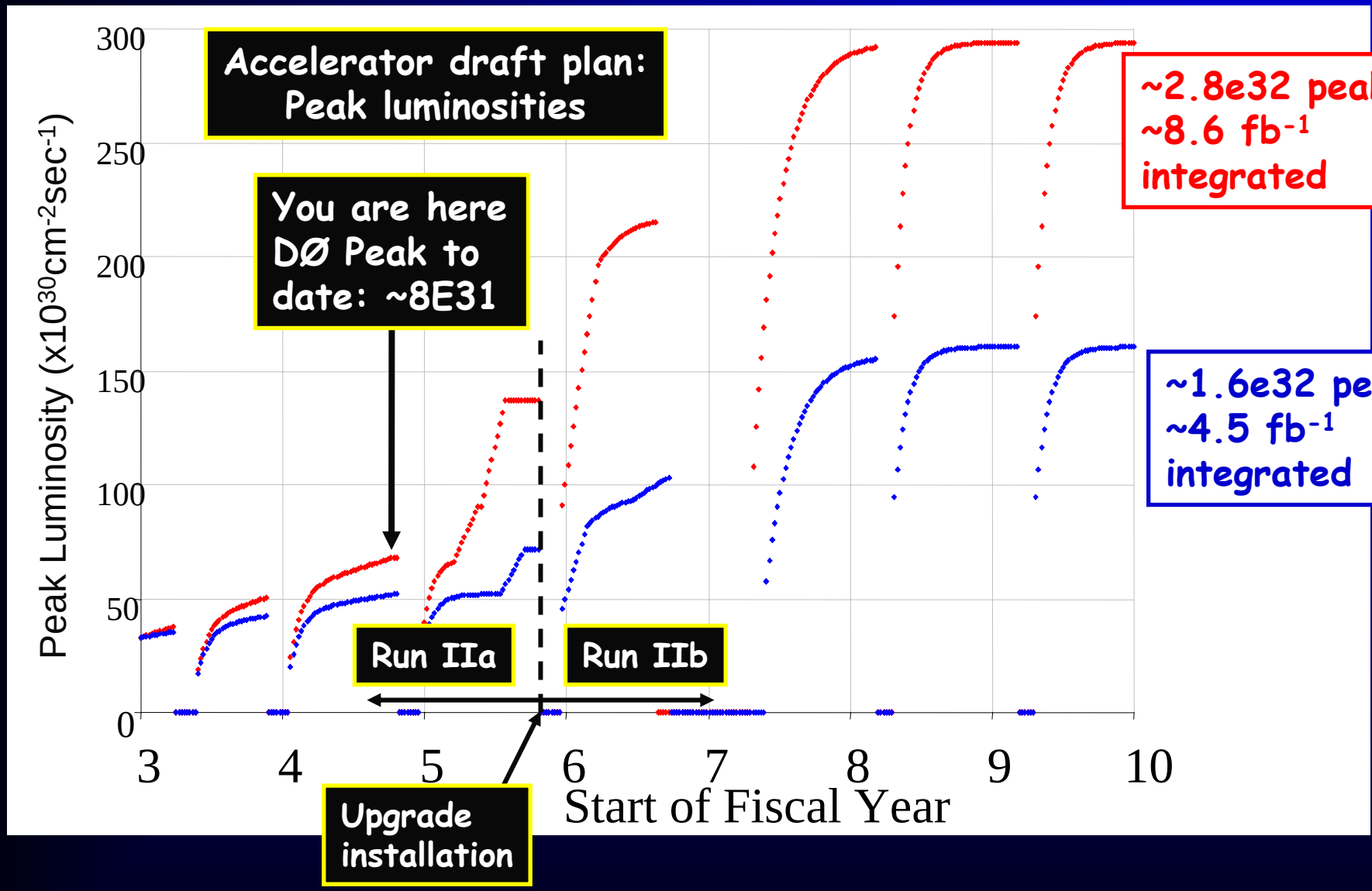
for the DØ Collaboration

DPF2004

The Need for Upgrades

- Run II at the Tevatron was originally planned to reach 2 fb^{-1}
- Physics (Higgs) potential indicated by the TeV2000 and TeV33 studies led to a revised goal of 15 fb^{-1} (subsequently adjusted to 8 fb^{-1} after 2003 Lehman Review)
  - Silicon detectors will not survive the corresponding integrated radiation dose
    - DØ: Inner layer will likely die from radiation damage at ~4 fb^{-1}
  - Trigger and DAQ systems will not be able to handle the high rates and occupancies
    - DØ: Estimate 30 kHz out of L1 trigger (currently 1.5 kHz)
    - 5 minimum bias interaction per crossing (currently 1)
- Upgrade programs for DØ and CDF were approved in 2002 (rescoped in 2003, including cancellation of silicon detector replacements)

Run II Luminosity Projections



Current Performance

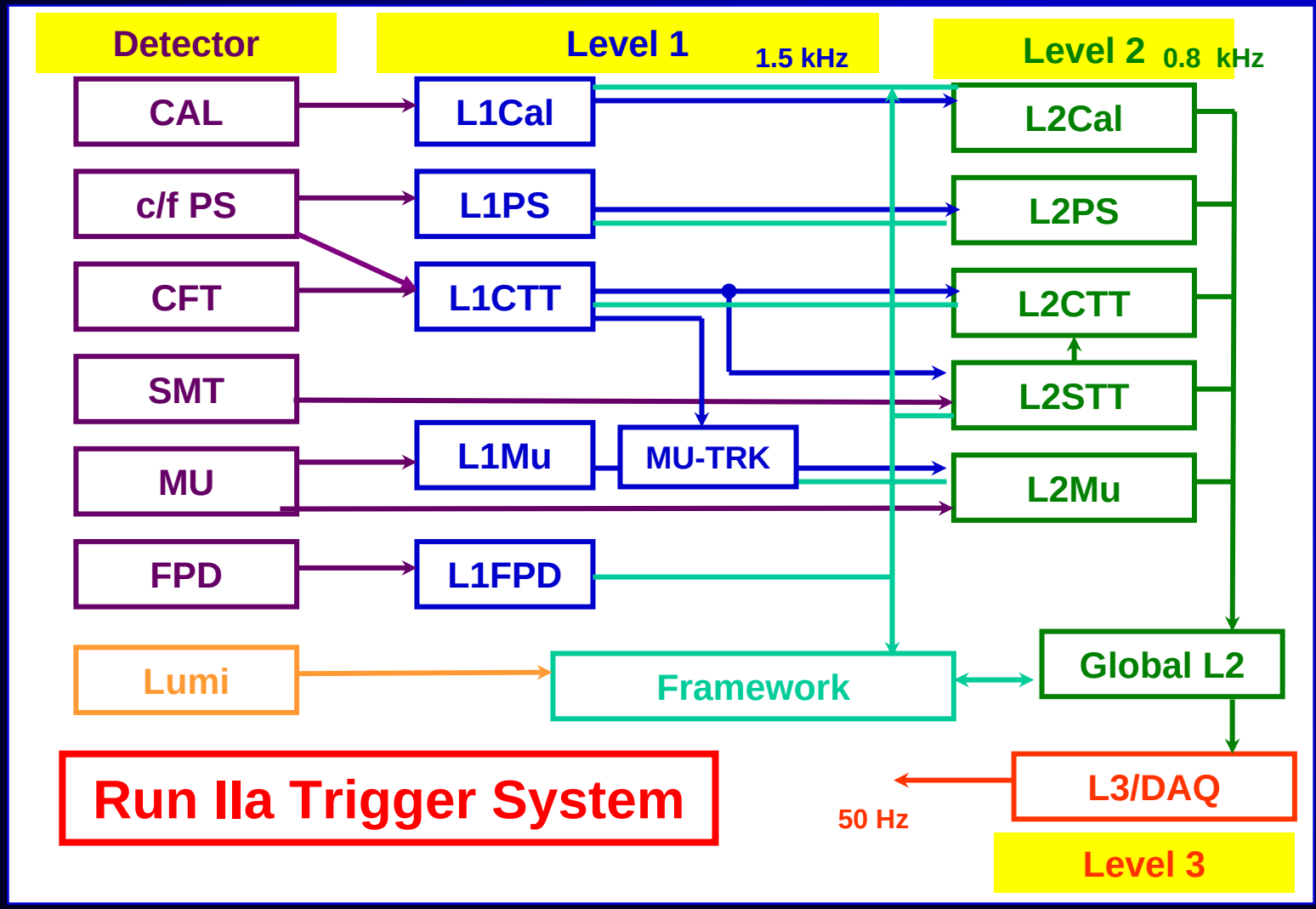
- Tevatron is now performing quite well
  - Running slightly ahead of design goals this year
    - ~9e31 peak luminosity
- Both detectors are working well and producing much good physics, but the improved accelerator performance is starting to expose the detectors' weaknesses
  - Difficulty meeting L1 accept goals
  - Tracking detector problems
  - Occupancy-related trigger rate issues
- We need quick and efficient commissioning of trigger and detector upgrades to address these issues

DØ Run IIb Upgrades

- **Goal:** maximize the flow and quality of physics data in a high luminosity environment

DØ Run IIb Upgrades

- **Strategies: Increase trigger rejection at L1**



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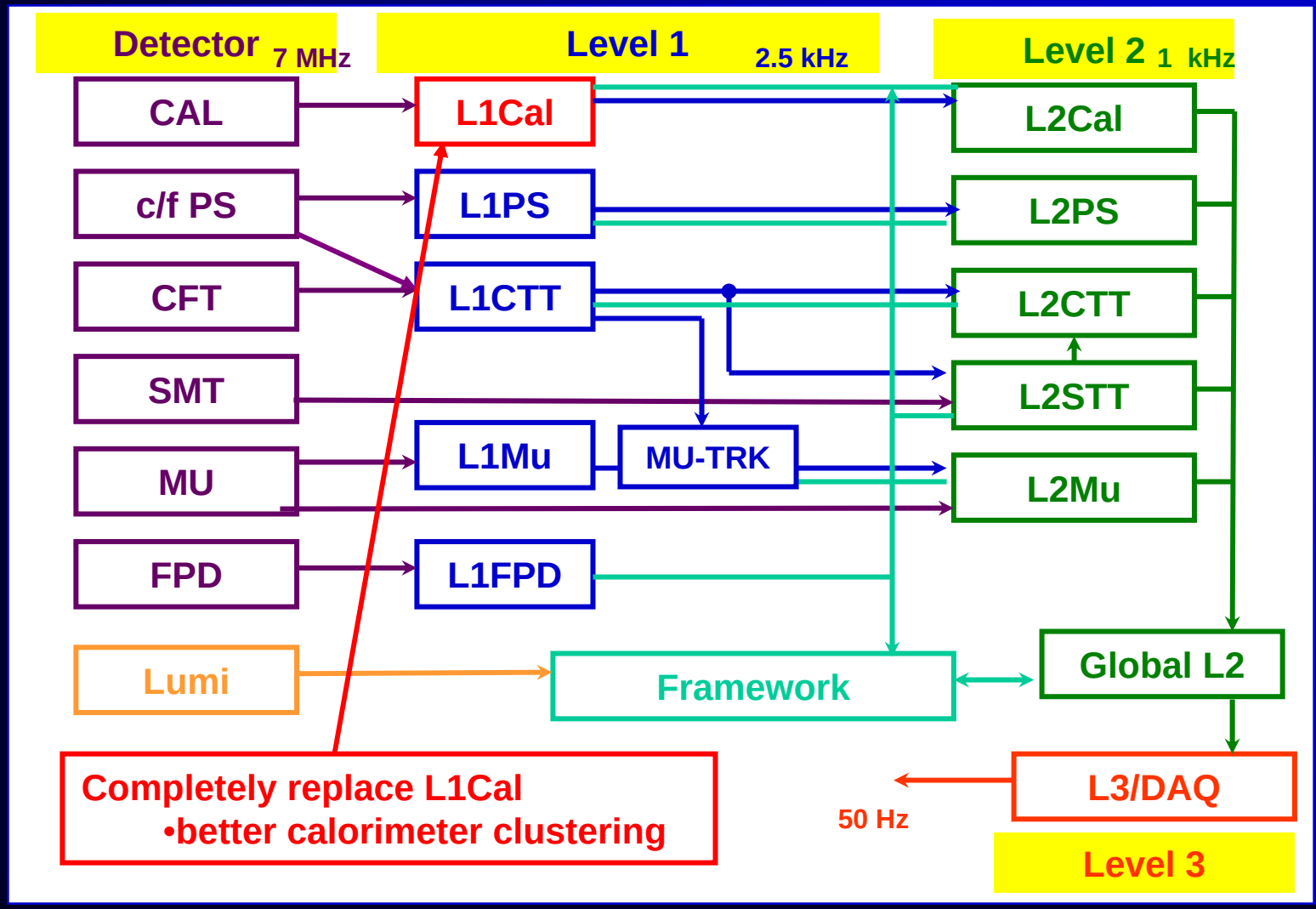

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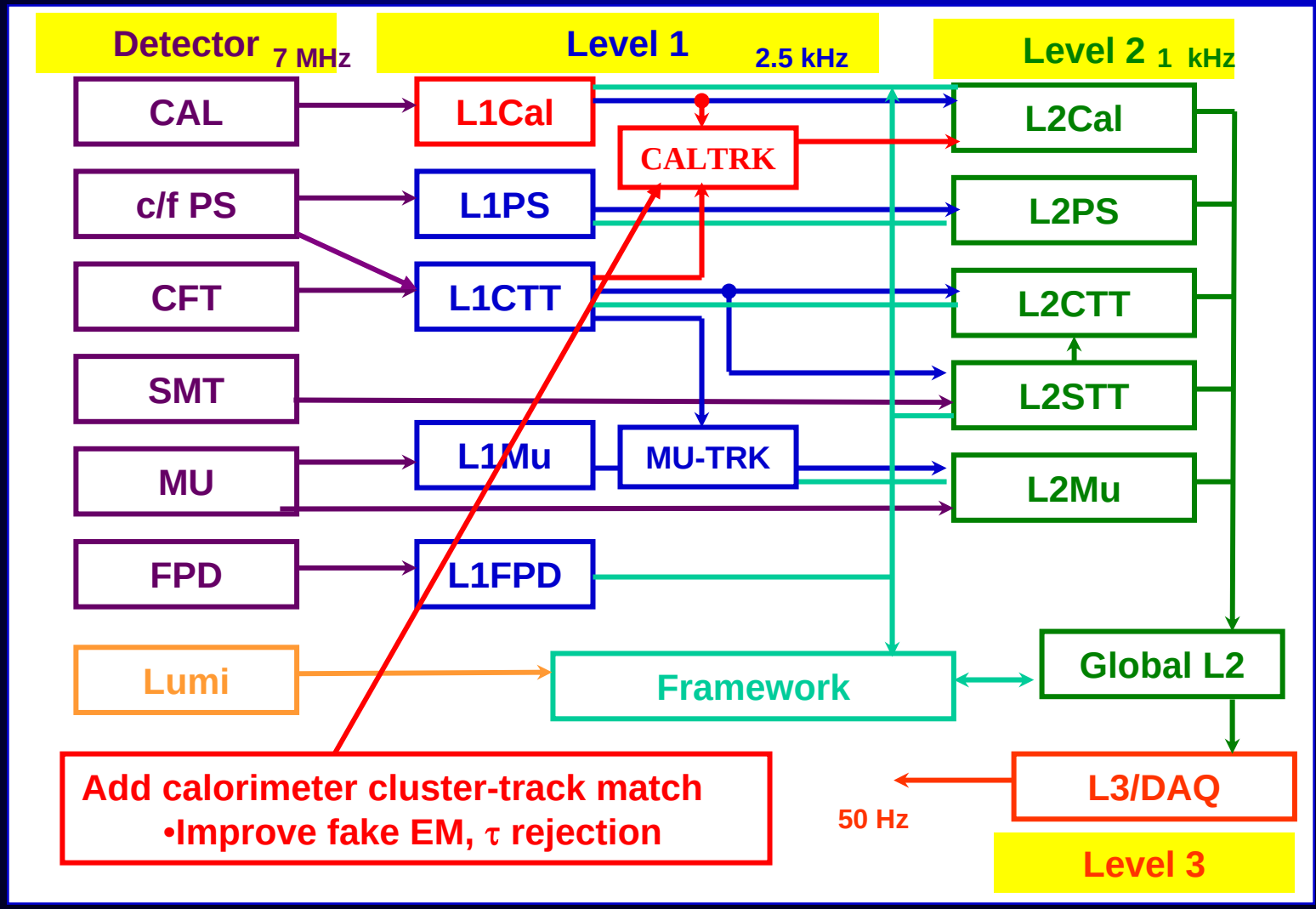

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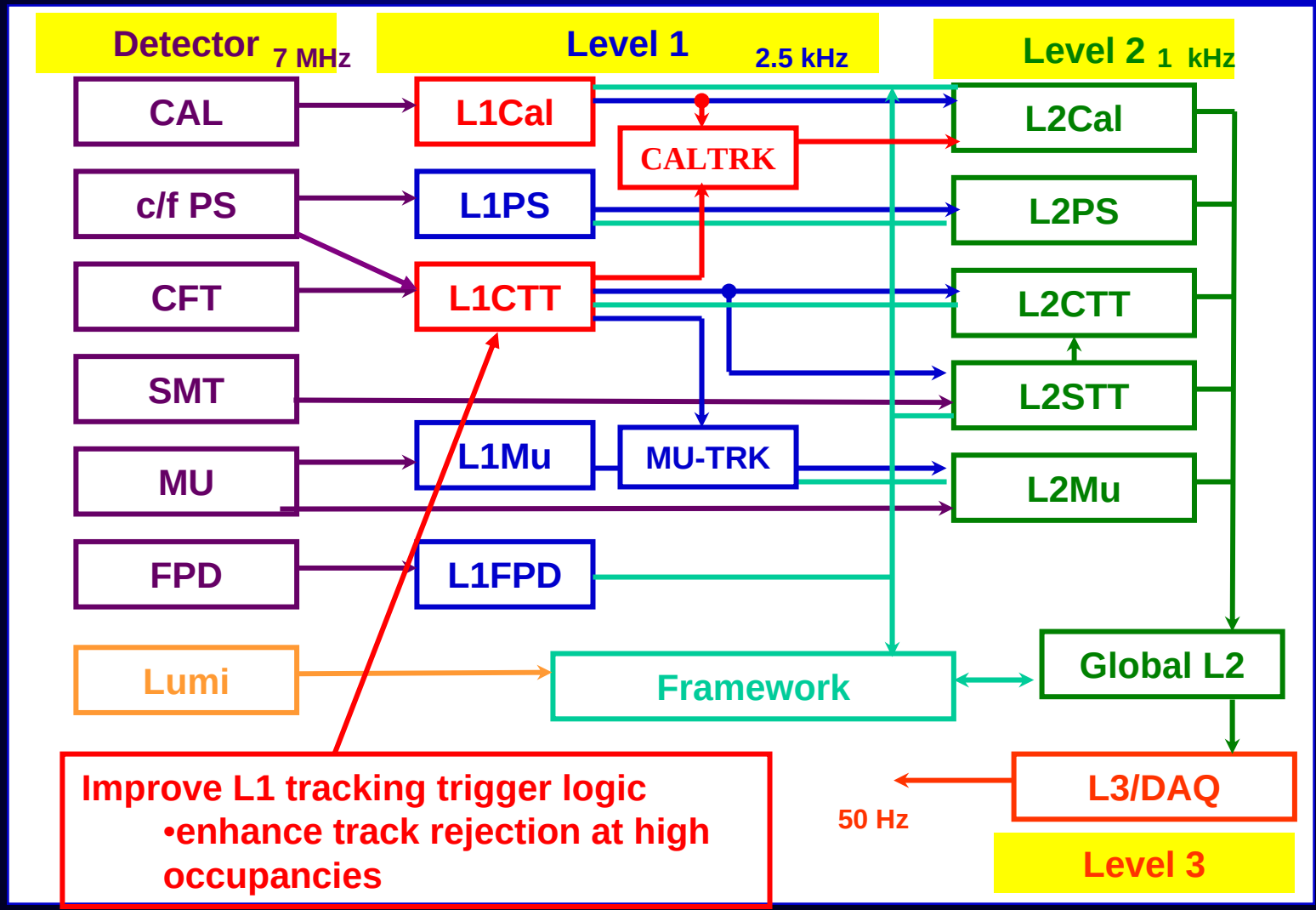

DØ Run IIb Upgrades

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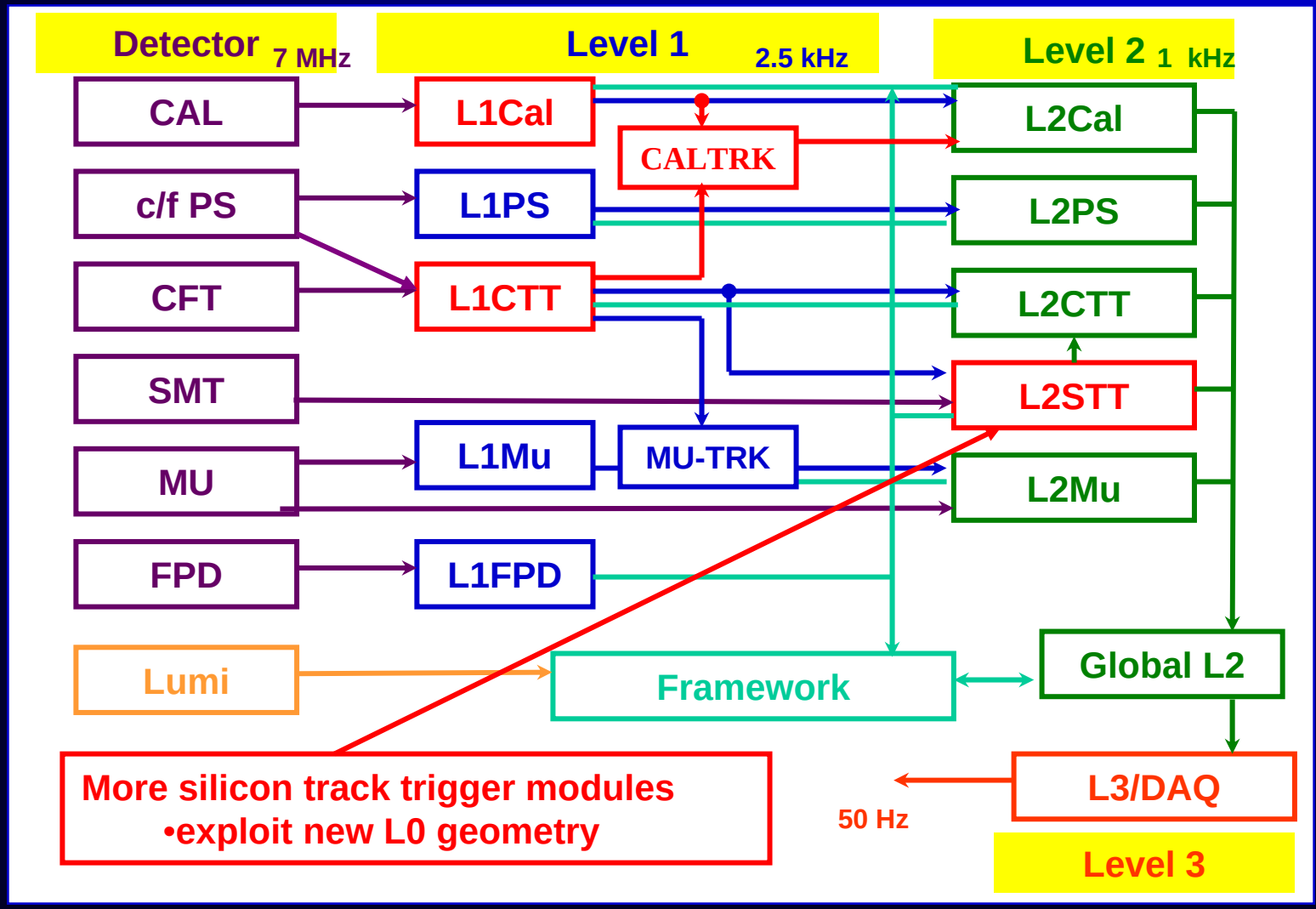

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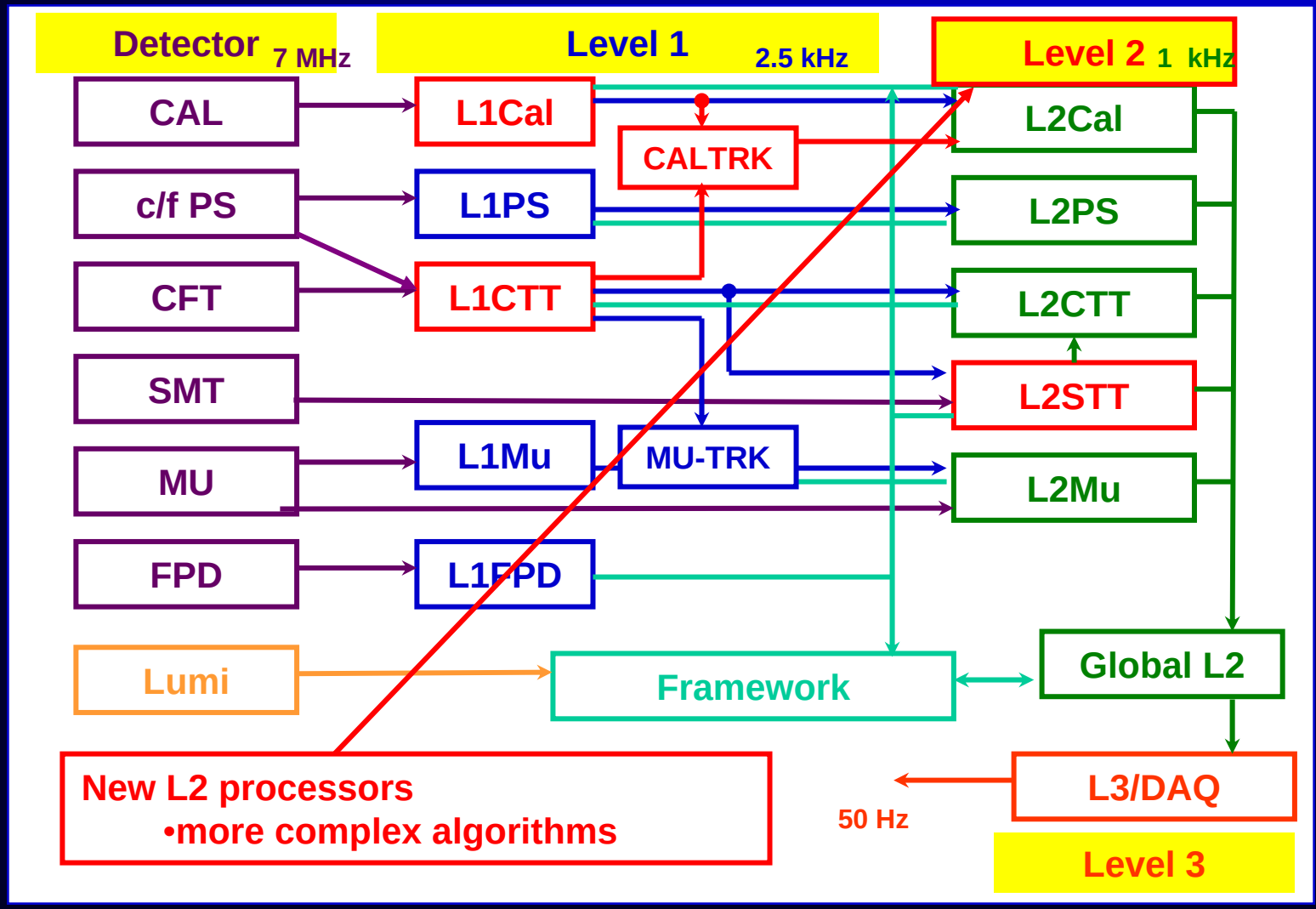
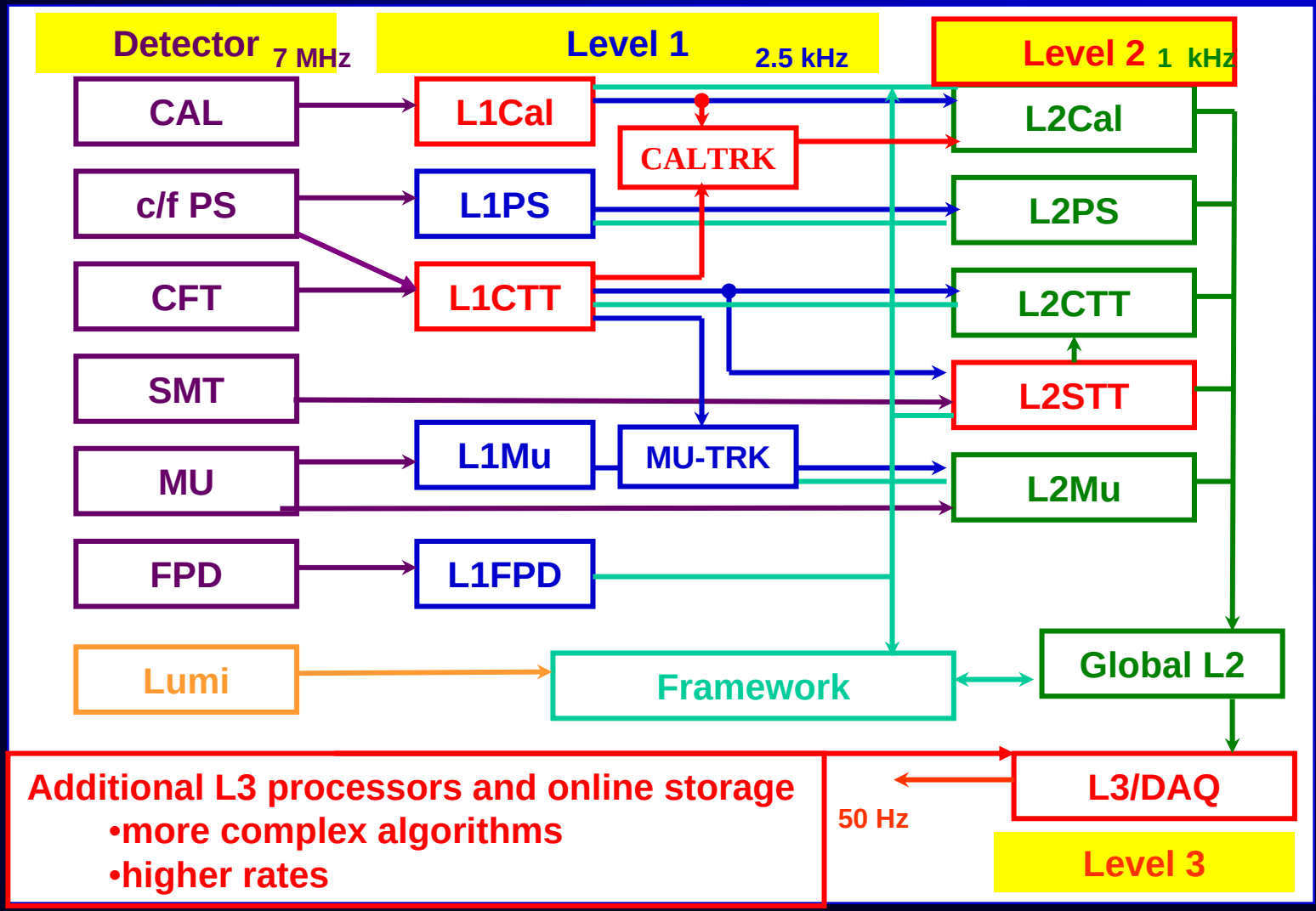


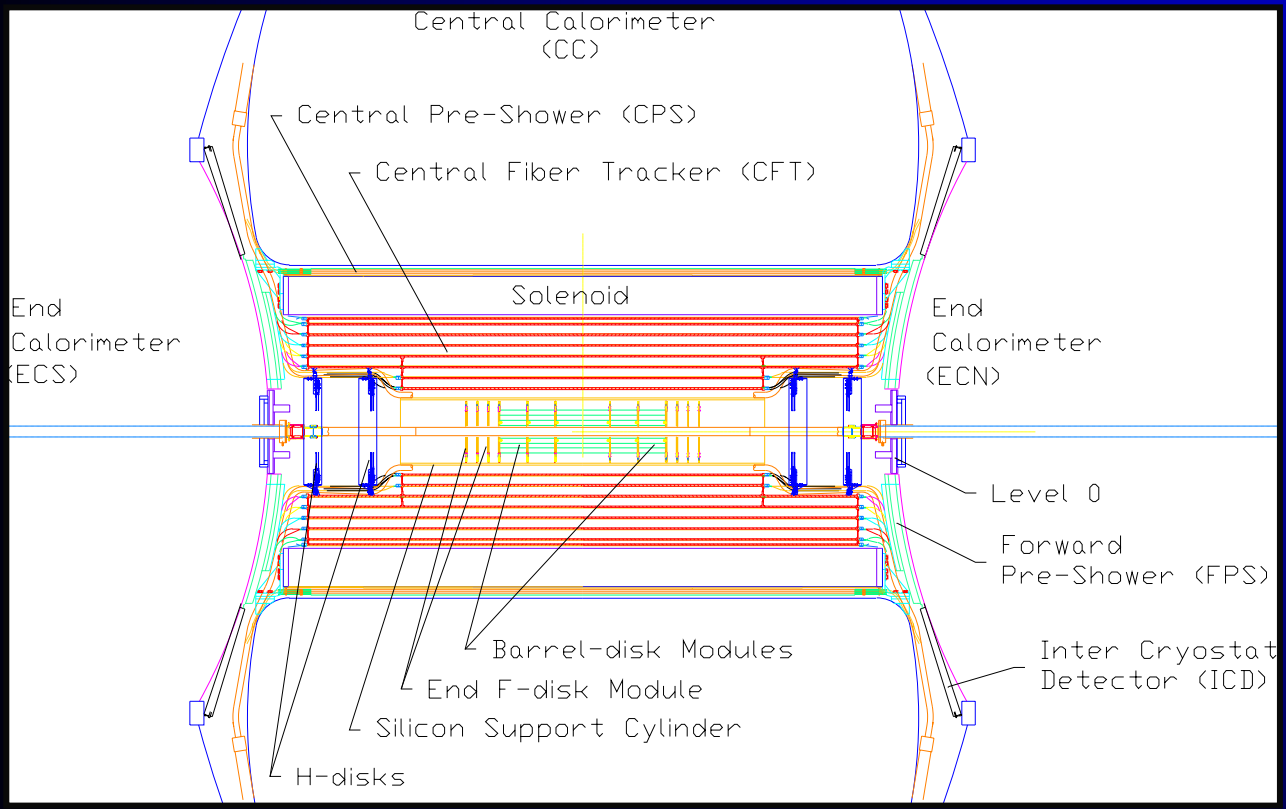
DØ Run IIb Upgrades

- **Strategies: More processing power at L3**



DØ Run IIb Upgrades

- **Strategies: Improve detector performance**



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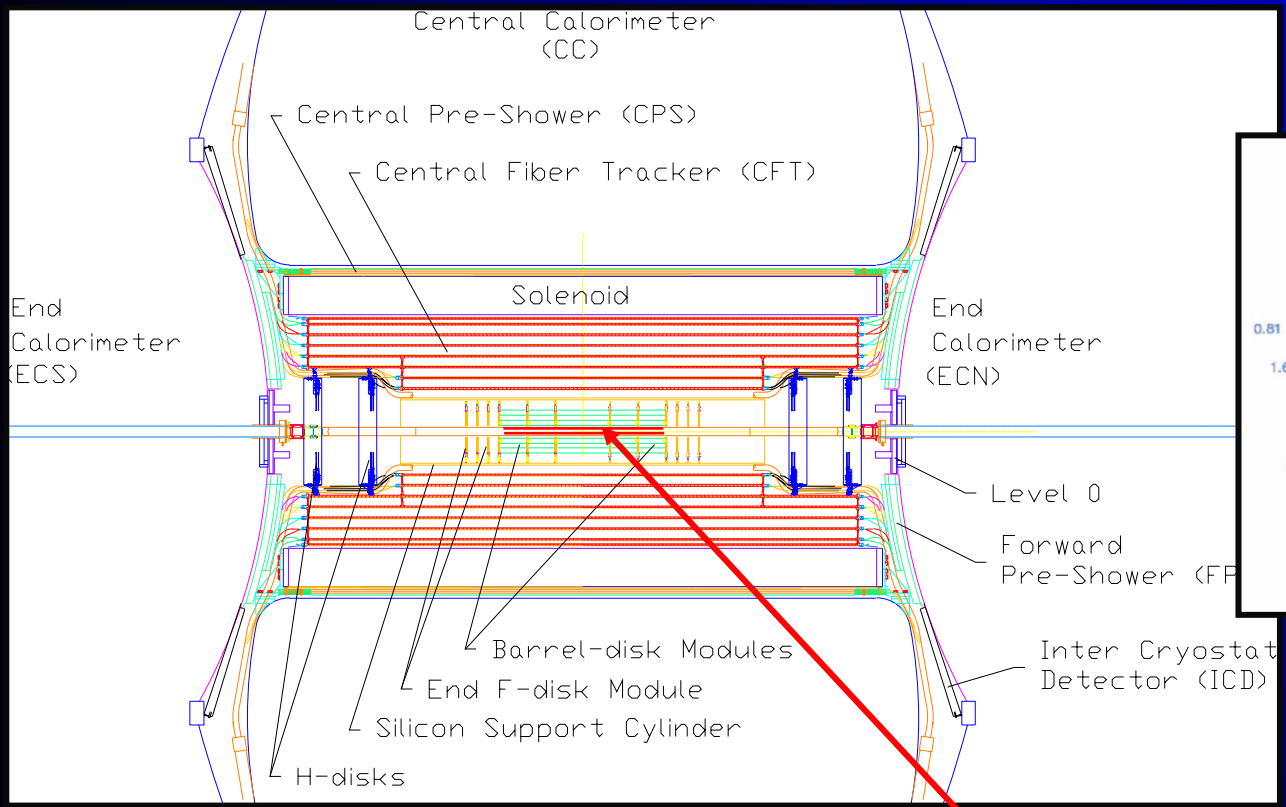

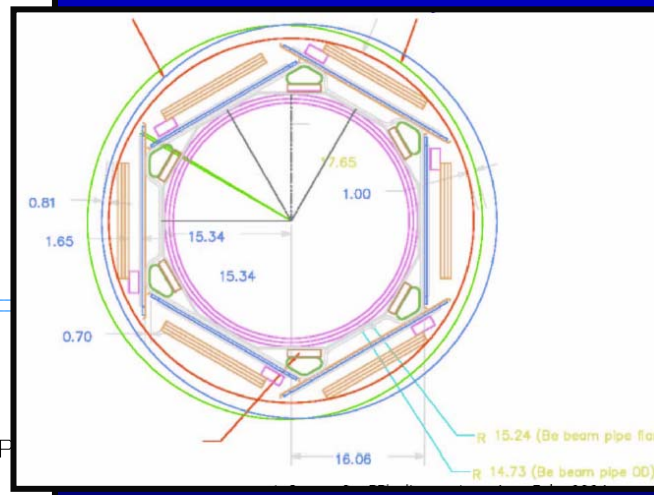

Layer 0: Additional inner silicon layer at small R (~1.6 cm)

- **Recover tracking,B-ID losses from rad damage and aging**
- **Improve impact parameter resolution**

DØ Run IIb Upgrades

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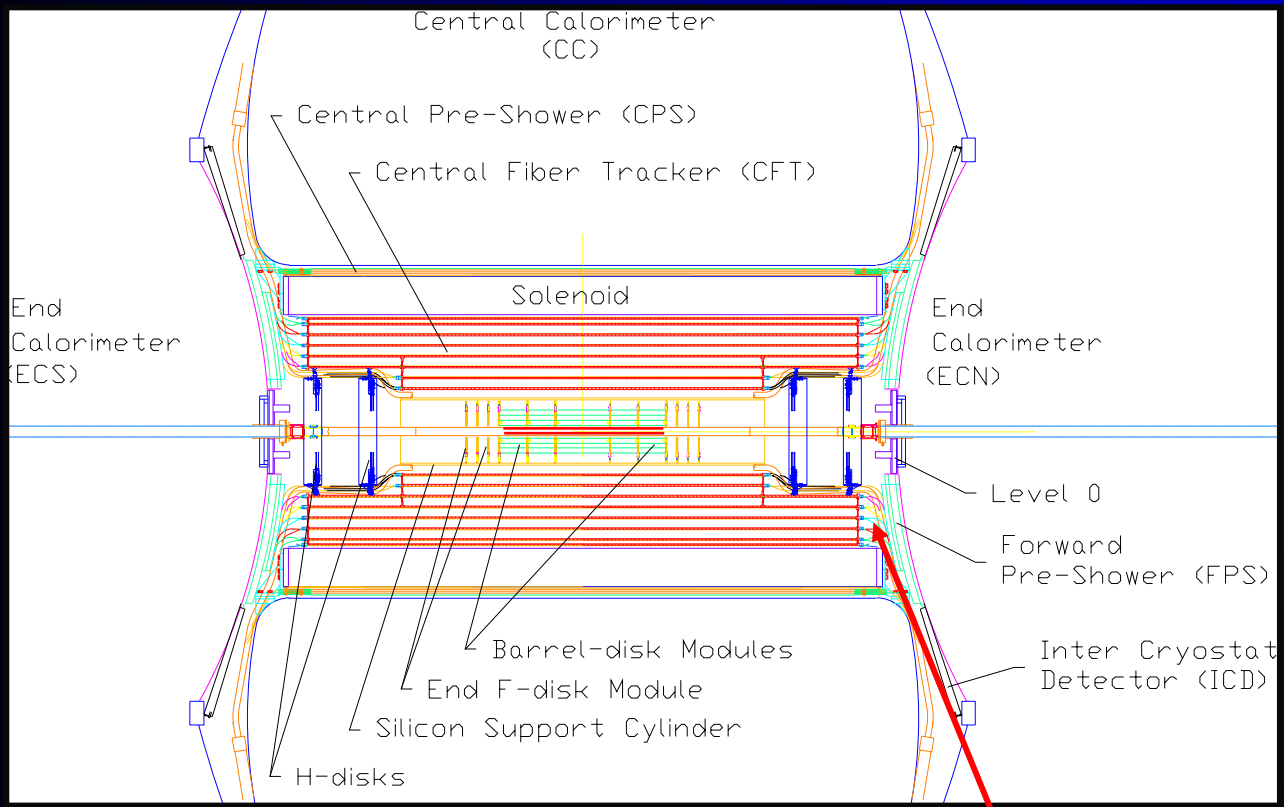
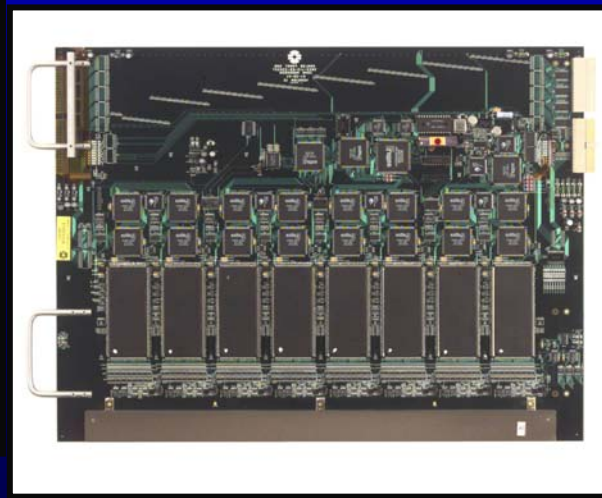
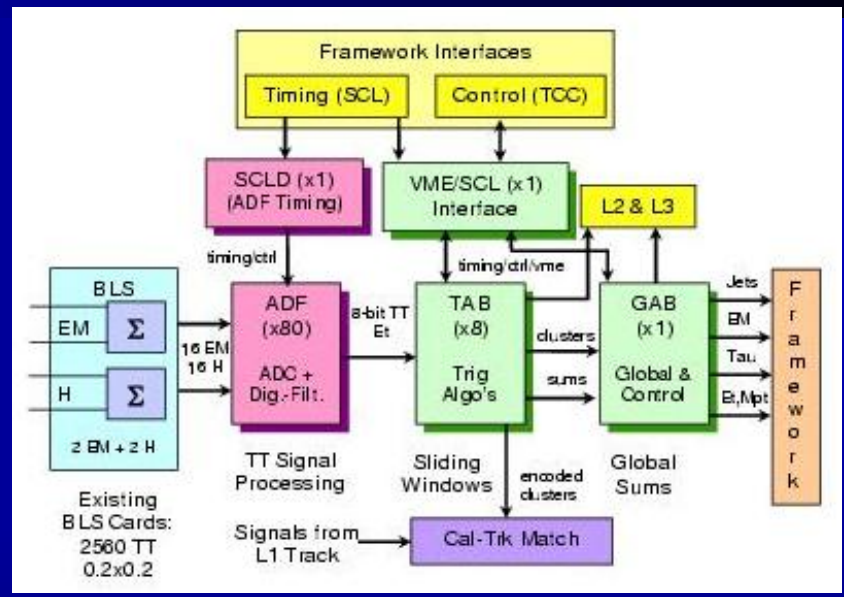




AFE II: New readout electronics for Central Fiber Tracker
•Improve tracking efficiency at high luminosity

Calorimeter Trigger Upgrade: L1CAL

- Biggest trigger upgrade project
  - Entire existing L1CAL system will be replaced



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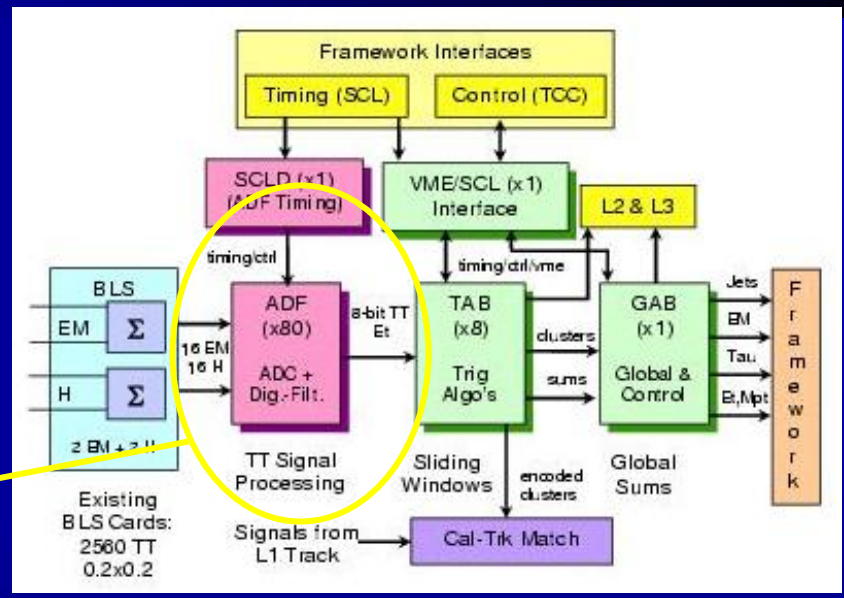

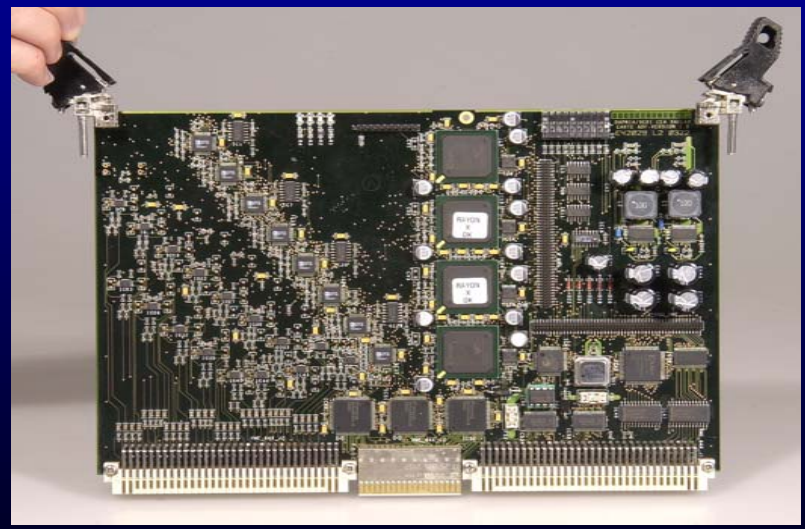

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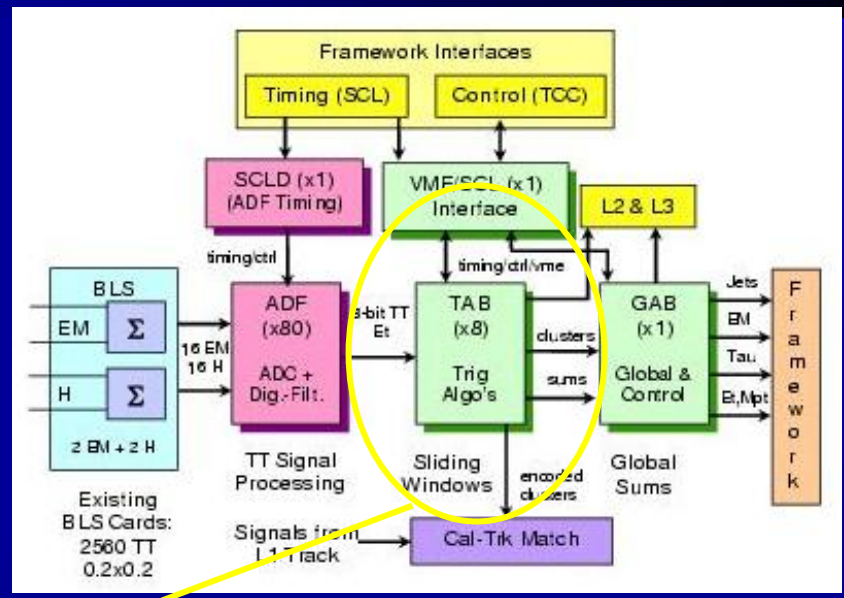
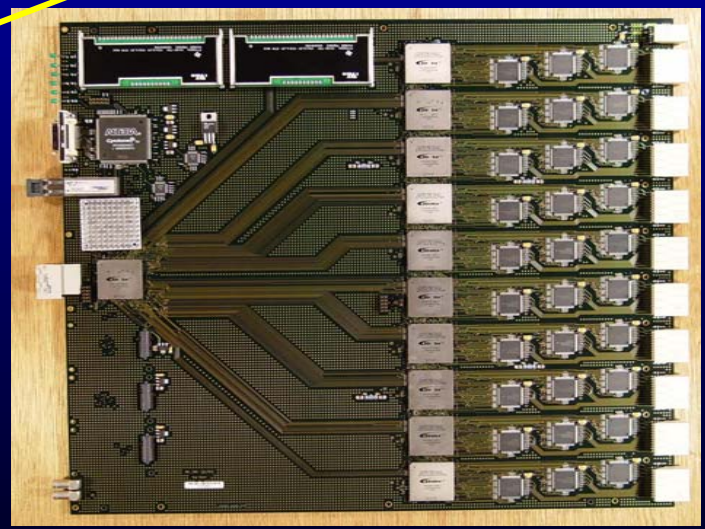
  - Better clustering to bring trigger rejection from L2 to L1





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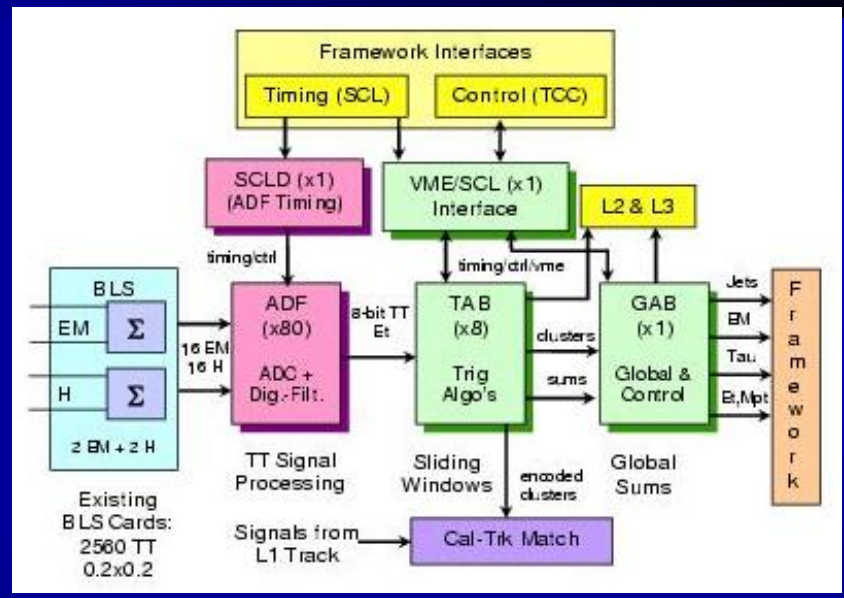
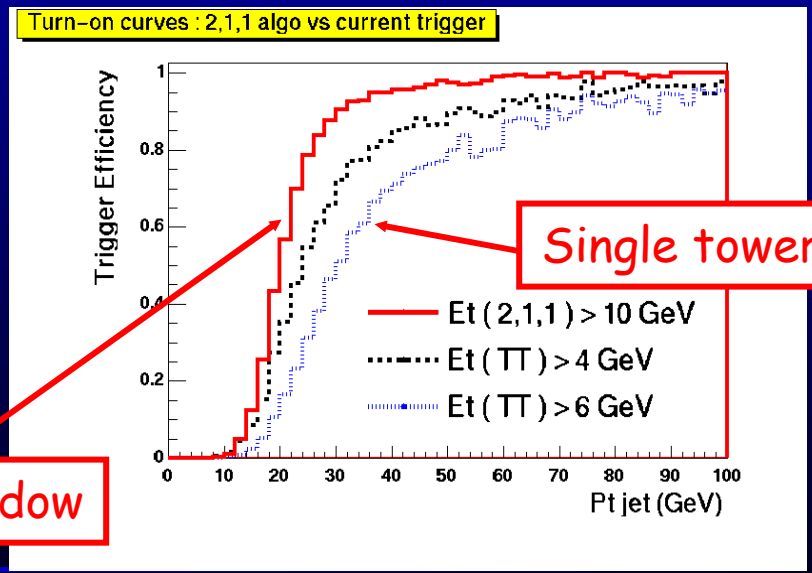
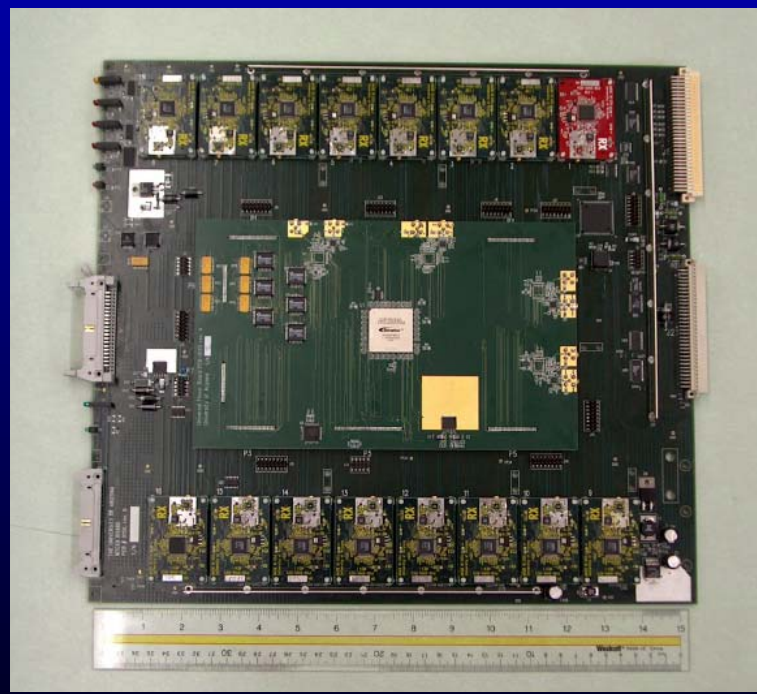
  - rejection from L2 to L1
- Trigger threshold turn-on is sharpened





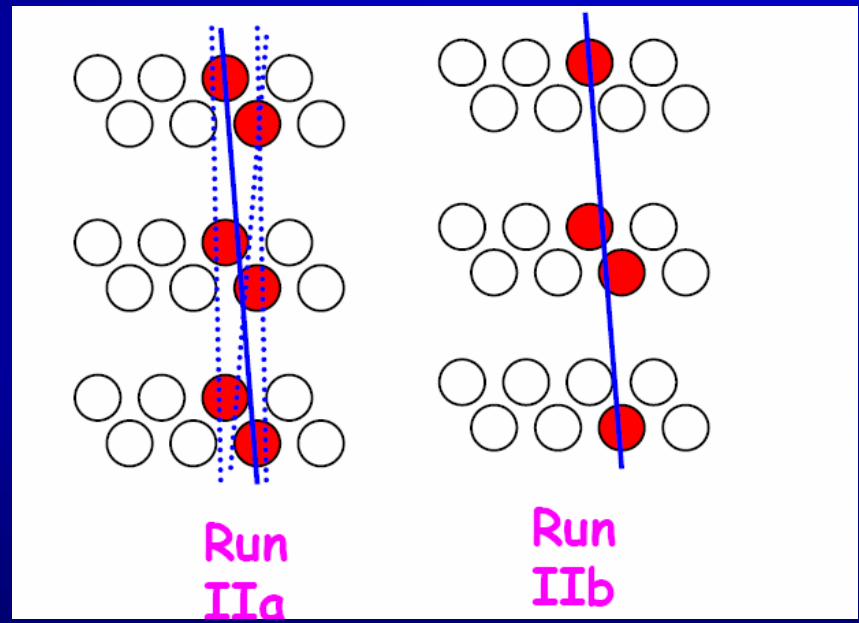
Calorimeter Track Match: L1CALTRK

- Match calorimeter clusters to CFT tracks
  - ϕ matching granularity improved x8
- Needed in triggers for Higgs searches
  - electrons in WH and $H \rightarrow W^*W$ modes
    - Fake EM rejection is improved by ~x2
  - taus in $H \rightarrow \tau\tau$ and $H^+ \rightarrow \tau\nu$
    - Fake τ rejection is improved by ~x10
- Implemented by making modest modifications to existing L1MUTRK hardware



L1 Central Track Trigger: L1CTT

- Provides tracks to L1MU and L2STT
  - Needed for triggering on *e*, μ, τ
- Run IIa L1CTT uses fiber doublet logic
- Upgrade uses fiber singlets to reduce combinatorics



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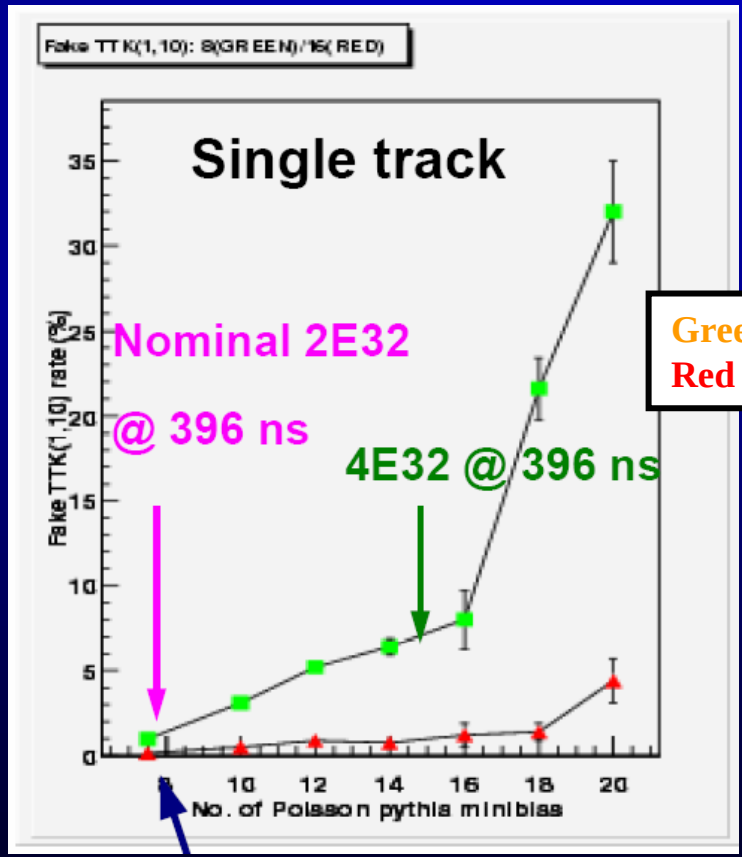
Fake Track Rate vs. Number of Min Bias (luminosity)



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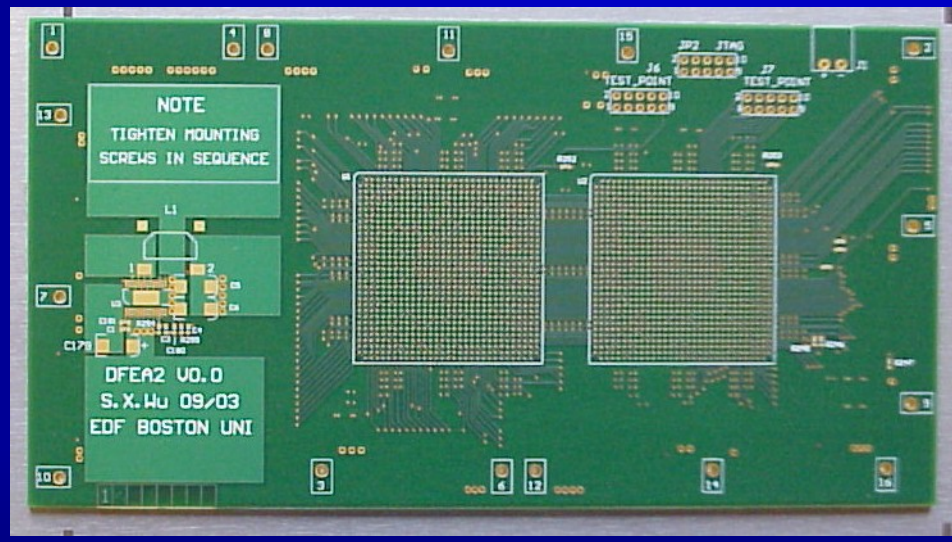
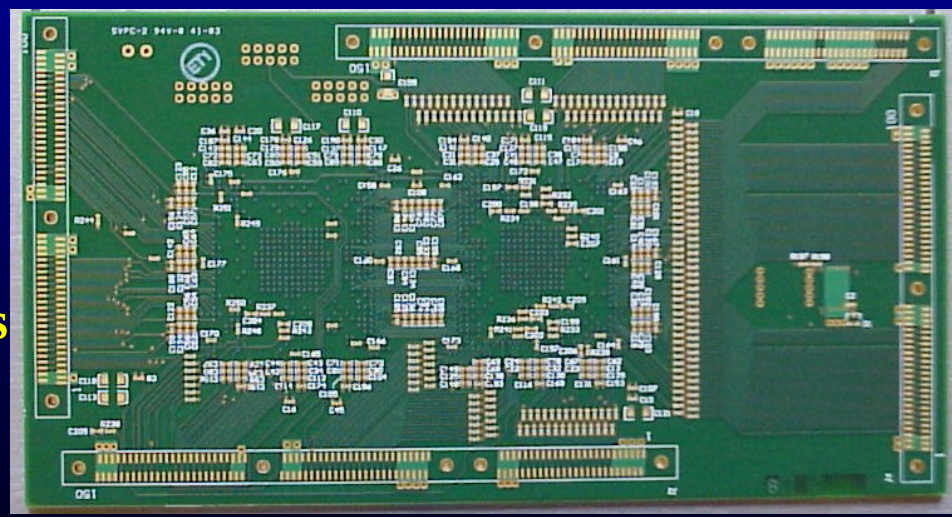
- Two crates of electronics will be replaced
  - New Digital Front End Axial (DFEA) cards with larger FPGA's for more complex algorithms using singlet logic

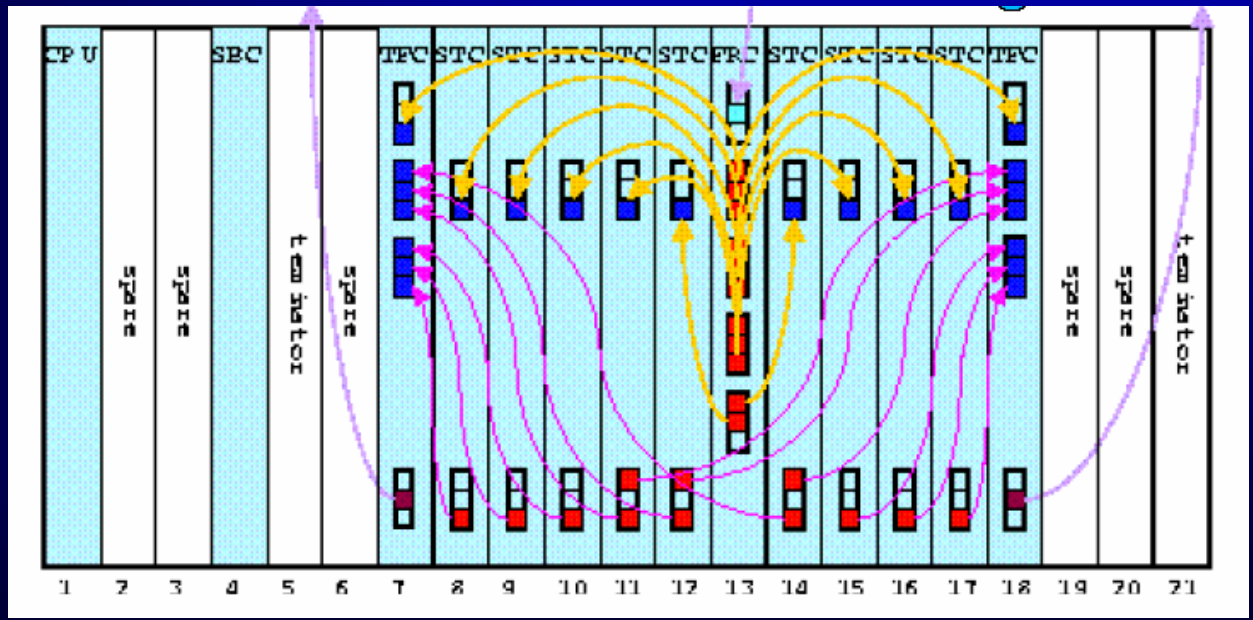
DFEA prototypes





L2 Trigger Upgrades

- Silicon Track Trigger: L2STT
  - Expand L2STT by installing additional Silicon Trigger Cards (STC - identical to existing cards) to handle inputs from new Layer 0 silicon channels



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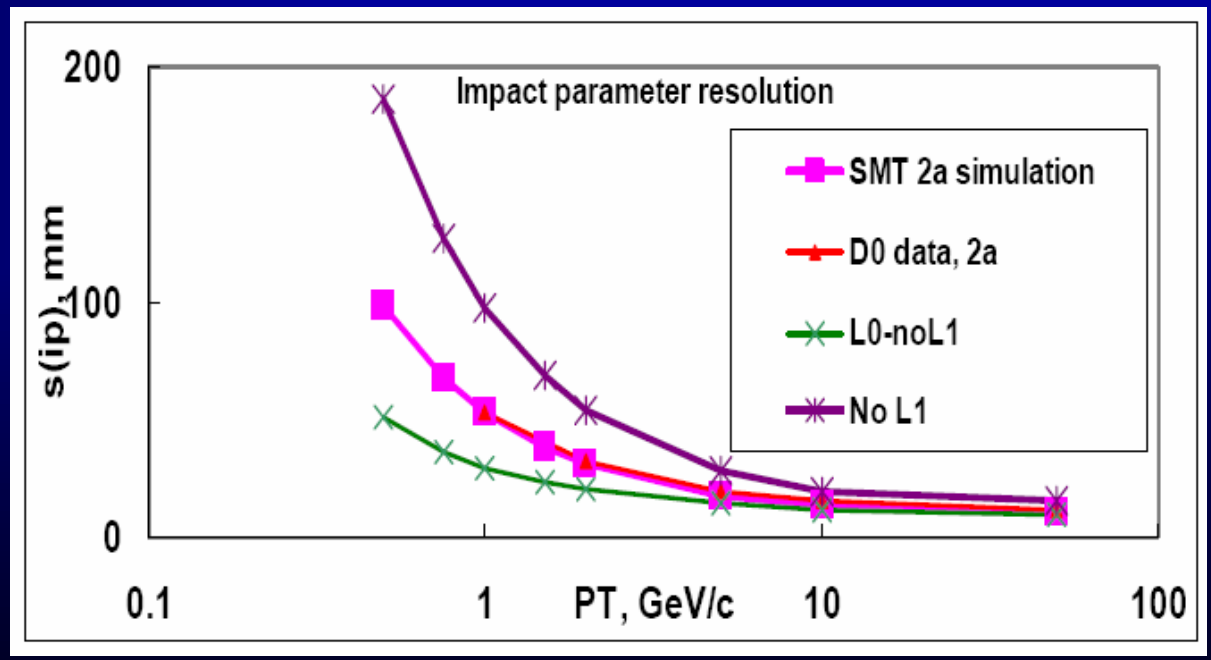
  - **Expand L2STT by installing additional Silicon Trigger Cards (STC - identical to existing cards) to handle inputs from new Layer 0 silicon channels**
- **L2 Processors: L2β**
  - **L2 Trigger systems use SBC processors**
  - **Began with Alpha-based custom boards**
  - **Upgrading to more powerful "L2-beta" processors**
    - **More complex algorithms for background rejection**

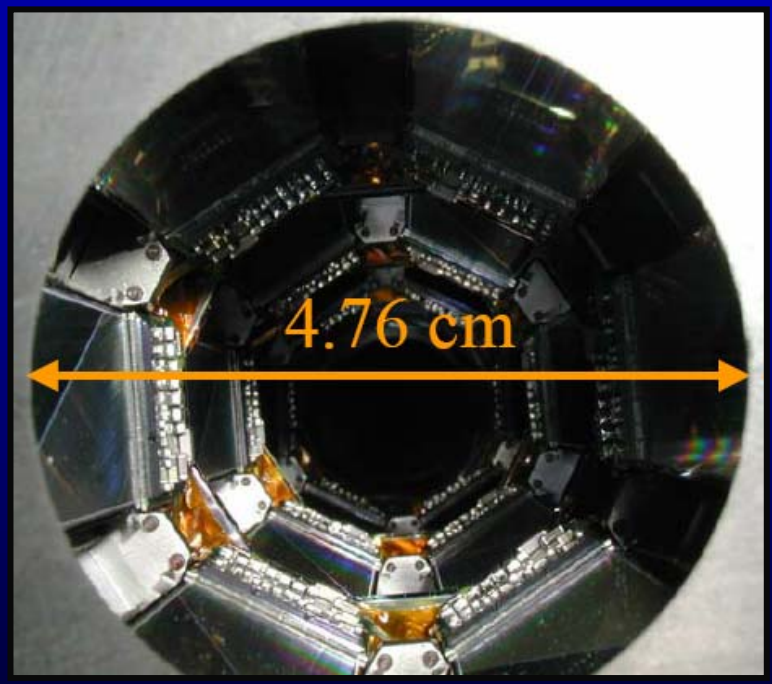
Layer 0 Silicon

- After Run IIb silicon upgrades were canceled, DØ proposed installing an inner layer silicon detector inside the Run IIa SMT
- Benefits of Layer 0
  - Recover tracking and B-ID losses from radiation damage and from aging
  - Enhance tracking and pattern recognition at high luminosity
  - Improve impact parameter resolution
    - Corresponding to 15% increase in b-tagging



Layer 0 Silicon

- Layer 0 makes very good use of much of the work done for the original silicon upgrade
  - R&D, SVX4 readout chip, carbon fiber support structure, beam pipe, etc.
- 1 layer of 48 silicon devices, 6-fold geometry, r~1.6 cm, mounted on the beam pipe
- Two of the toughest challenges
  - Mechanical and electrical constraints fitting between the beam pipe and Run IIa SMT
    - Beam region apertures are being re-surveyed during current shutdown



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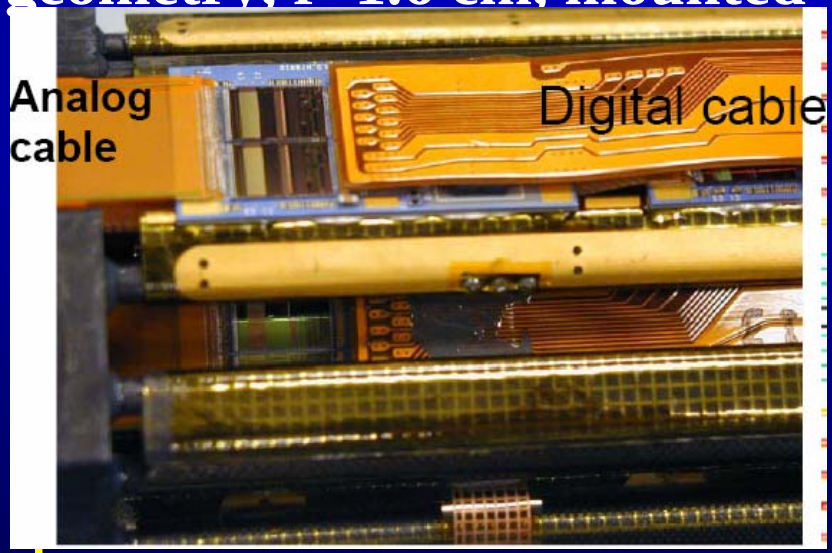
  - Noise problems from analog cables in close proximity to conducting support surfaces and ground loops
    - Novel grounding scheme with laminated ground mesh covering all CF surfaces. Excellent noise performance with no Faraday cage.



Other Upgrades

- DAQ/Online computing
  - 96 new Linux nodes for the L3 farm
    - From 322 to 659 "GHz equivalent" nodes
      - Ability to efficiently process more complex high lumi events
      - Increase L2 accept from 850 to 1000 Hz
  - Database, file servers, data loggers being moved from AlphaServer to Linux cluster
  - Upgrade critical control system processors with next generation PowerPCs running VxWorks
- AFEII: new readout electronics for Fiber Tracker
  - Problems with AFEI associated with chips (SIFT-SVXIIe)
    - e.g. threshold limitations
  - AFEII boards would use new pipeline/trigger chip (TriP-TriPt)
  - Improve tracking efficiency at high luminosity
  - Conditionally approved: Lab review expected 2/05

Upgrade Status

- In general,
  - Hardware: mostly in good shape and progressing on schedule
  - Software: mostly just getting started – a lot of work to do
- A few notes…
  - L1CAL: ADC & Digital Filter board (ADF) version 2 prototype layout underway
  - L1CTT: Recent upscope in project – redesigned to make commissioning easier – new DFEA board has been laid out
  - Layer 0: module production starts this fall ahead of schedule
  - AFEII: prototype testing 9/04, internal review 1/05, Director's review 2/05
  - Everything else: pretty smooth sailing

Final Words

- DØ Trigger and Layer 0 upgrade projects are maintaining very aggressive schedules
  - Trigger systems are all in prototype testing or ready for production order
  - Layer 0 on schedule for early module production
- Much attention is starting to be focused on software and physics commissioning
  - Get back to physics quality data taking as quickly as possible once the upgrades are installed
    - Standing Committee on Upgrade Installation to Physics Commissioning (SCIPC): 16 member group charged to address this specific issue