Design, Preproduction, and Performance of the CDF Run IIb Silicon Detector

Paul Lujan

Lawrence Berkeley National Laboratory

DPF 2004

History of Run IIb

- Current silicon detector (SVXII and L00) was not expected to survive radiation generated by luminosity in Tevatron Run II
- Upgrade necessary to preserve functionality of the silicon detector
- Cancelled in September 2003 due to lowered luminosity projections for Run II
- We finished preproduction and present results

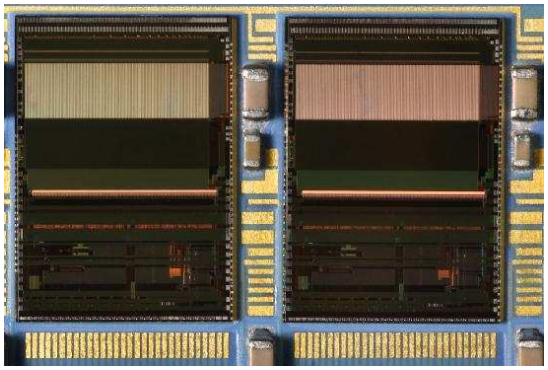
Design Issues and Solutions

- Current chips (SVX3D) and double-sided sensors not able to tolerate high radiation dose
  - design new chip (SVX4) with superior tolerance; use single-sided, actively-cooled sensors to minimize leakage current and preserve full depletion
- Material budget must be minimized (especially with single-sided sensors)
  - use new "stave" design and new layer arrangement to produce a compact, efficient structure (except innermost layer, L0)
  - stave design also means only one hybrid and two sensor designs are required for staves, simplifying overall design
- Use new technologies developed for L00 and at LHC

The SVX4 Chip

- Overall, very similar functionality to the SVX3D which it replaces; 1 chip reads out 128 channels

Consists of two parts:



- An analog front-end, where a charge-integrating preamplifier integrates charge from the silicon sensor and stores it in a 46-cell-deep pipeline
- A digital back-end, which reads cells selected by L1 trigger from the pipeline, digitizes them using a Wilkinson-type ADC, and reads them out

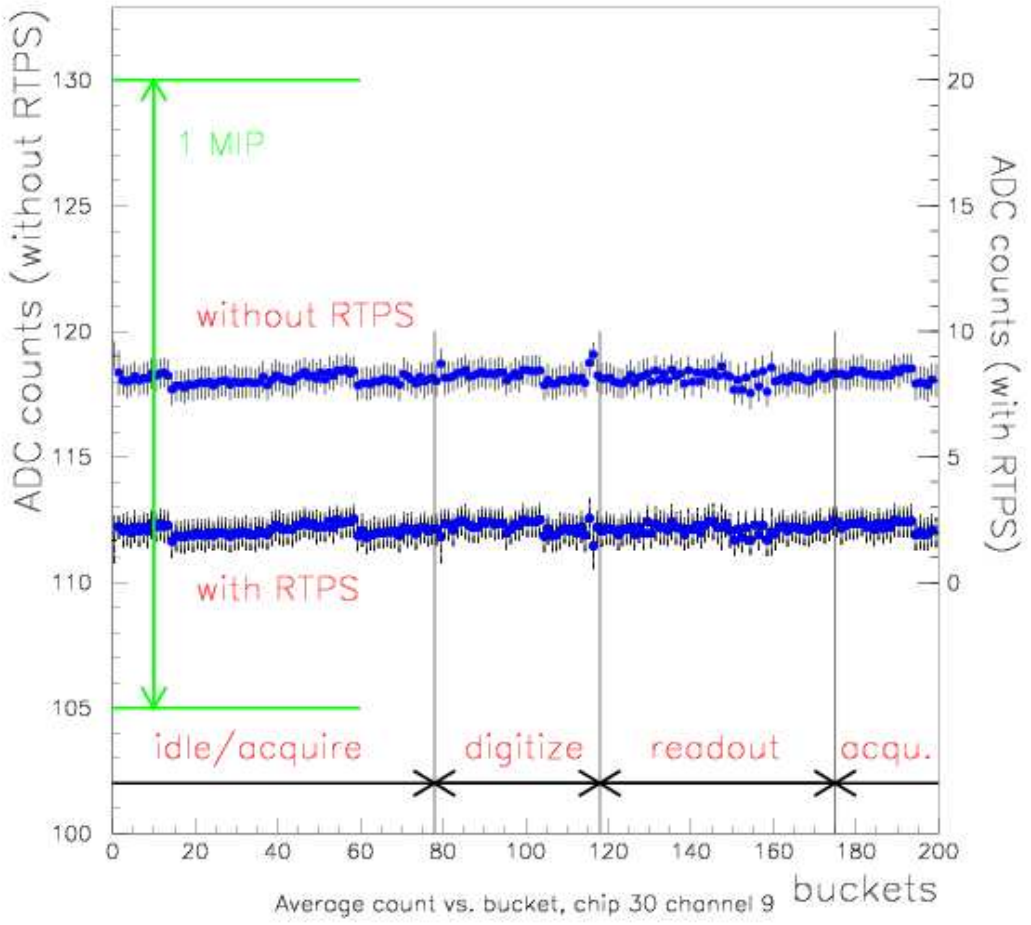
SVX4 Important Features

- Sparsification: read out only channels above configurable threshold
- Real-time pedestal subtraction (RTPS): subtracts average (common-mode) pedestal from all channels
- Deadtimeless performance: Front end continues to acquire data while back end is digitizing and reading out
  - Very important issue: we need to make sure that the data acquired by the front end is not affected by the activity of the back end

SVX4 Deadtimeless Performance

Overall, there is excellent front-end stability – a variation of at most 1-2 ADC counts during digitize or readout

(In Run IIa, 30% of all data was acquired during digitize or readout)



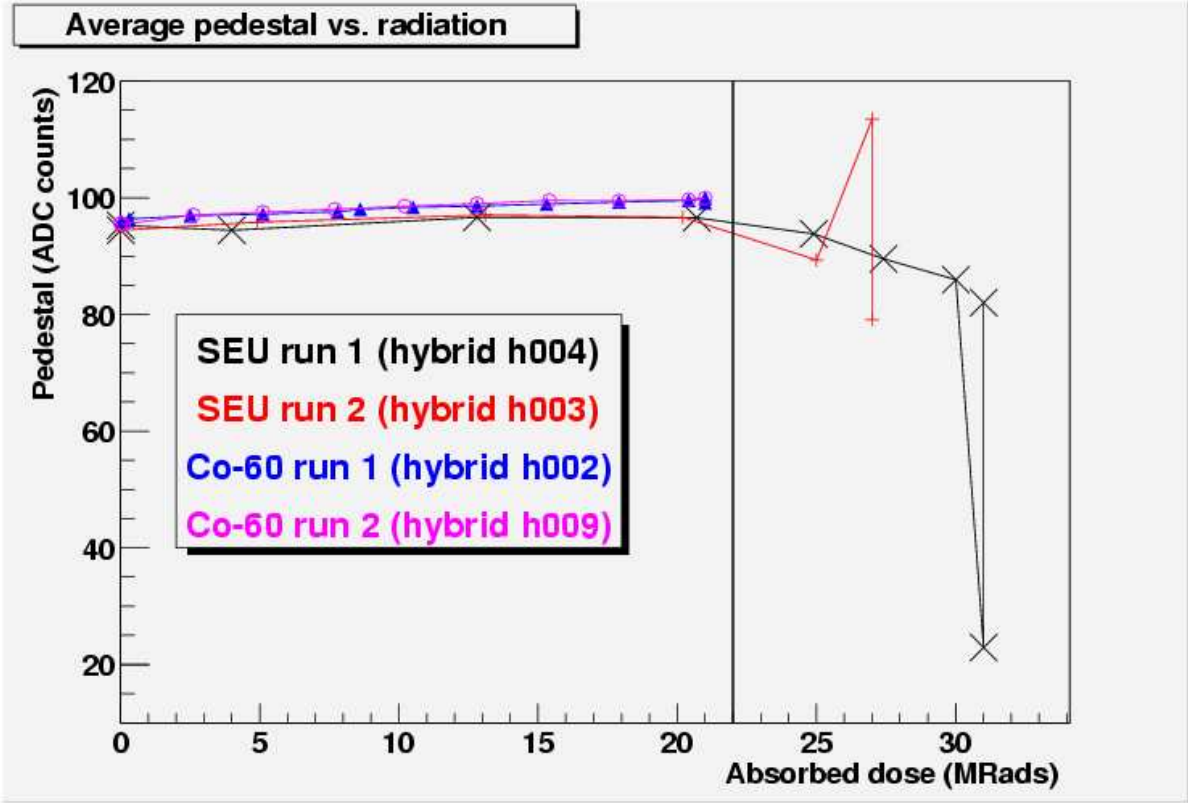
SVX4 vs. SVX3D

- Very similar functionality and performance, but:
- SVX3D used a custom 0.8 μm radiation-hard process from Honeywell
  - Greater expense, poor yield, guaranteed radiation tolerance of ~ 2 MRad
- SVX4 uses commercial 0.25 μm CMOS technology with "radiation-hard by design" layout principles (developed for LHC)
  - Cheaper, better yield, and radiation tolerance in excess of 20 MRad

Radiation tests of SVX4

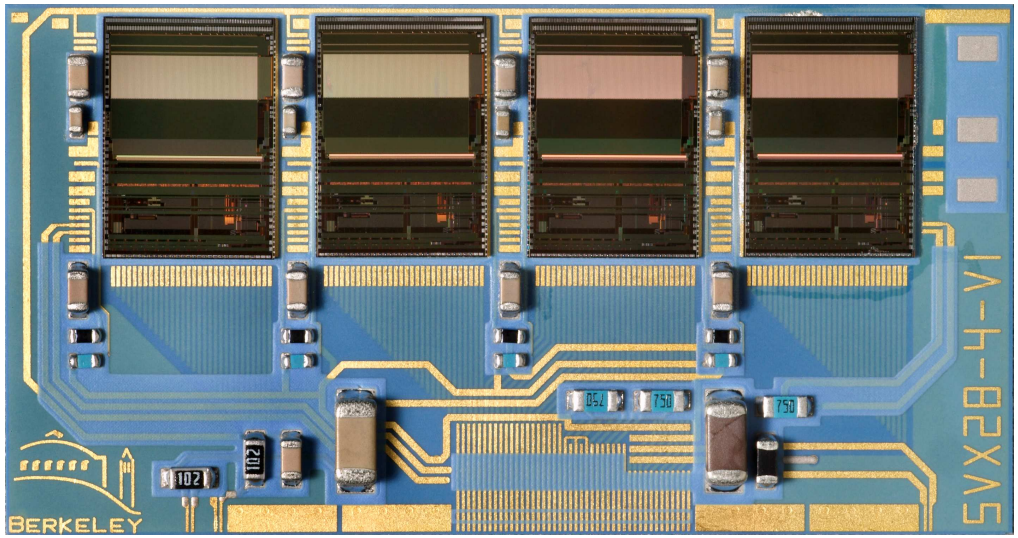
Four hybrids tested: two with Co-60 γ radiation, and two in the proton cyclotron at UC-Davis (also for SEUs).

No significant change in any performance parameters (pedestal, noise, gain, etc.) up to 20 MRad.



SVX4 Hybrids

- 4-chip hybrids for staves (also 2-chip hybrids for L0)
- BeO substrate (high thermal conductivity)
- traces printed using fine-pitch thick film technology (first used for L00 in SVXII)
- 100 μm-wide traces and 125 μm vias
- overall small size, light weight, and a total of 4 gold layers (less material)

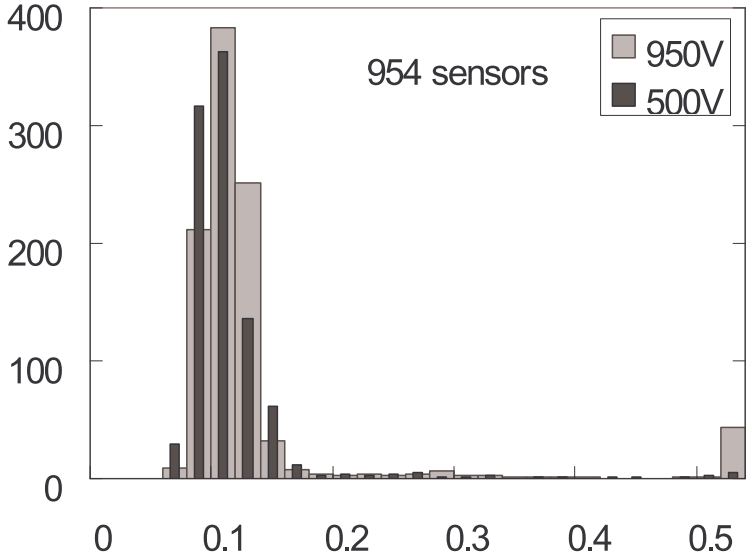


Preproduction Results

- Chips and hybrids met our performance goals
- Yields: Of 782 SVX4.2B chips tested, 617 (79%) were good or fair (0 or 1 bad capacitors, out of 5888 total; looser standards could have provided more chips total up to 89% yield)
- Of 117 hybrids produced, 108 (92%) passed initial testing, and 101 were burned in (all hybrids passed burn-in successfully)

Sensors

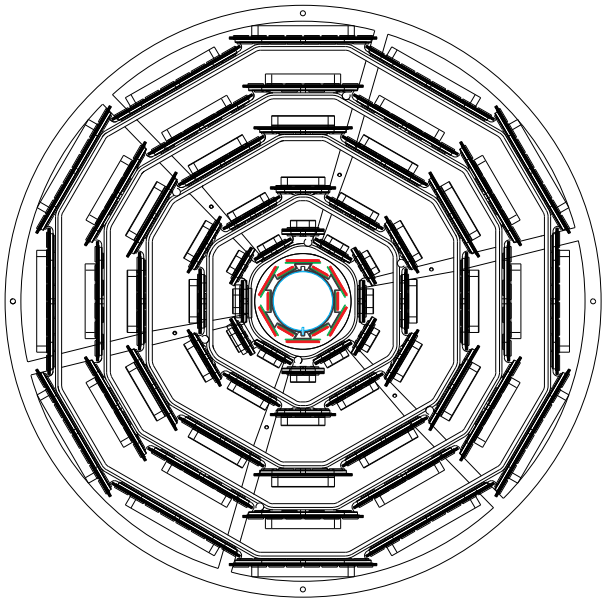
- Designed for high radiation hardness and high breakdown voltage
- Two types of sensors: axial and small-angle (1.2º) stereo (plus one narrow type for L0)
- <1% bad channel rate
- Active cooling: < -5º C for innermost sensors to minimize leakage current



Leakage current for sensors

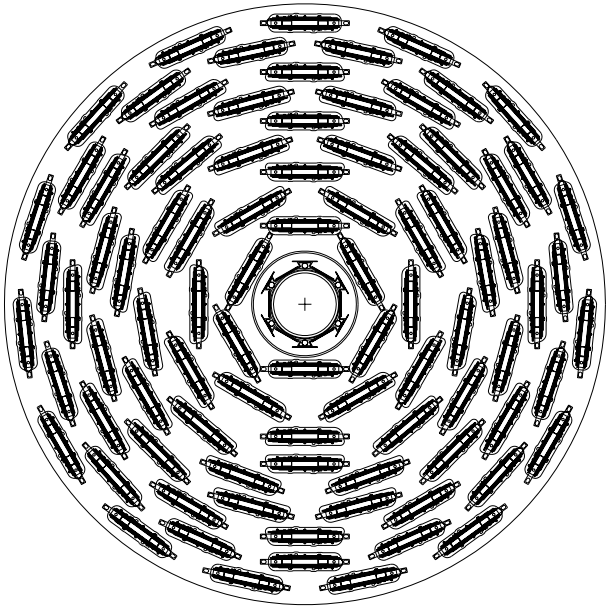
Layout: Run IIa vs. IIb

- Run IIa design divides into wedges, requiring separate sensor, ladder and hybrid designs for each layer
- Run IIb design uses single stave size for all layers, simplifying design (at the cost of a slightly more complex geometry)

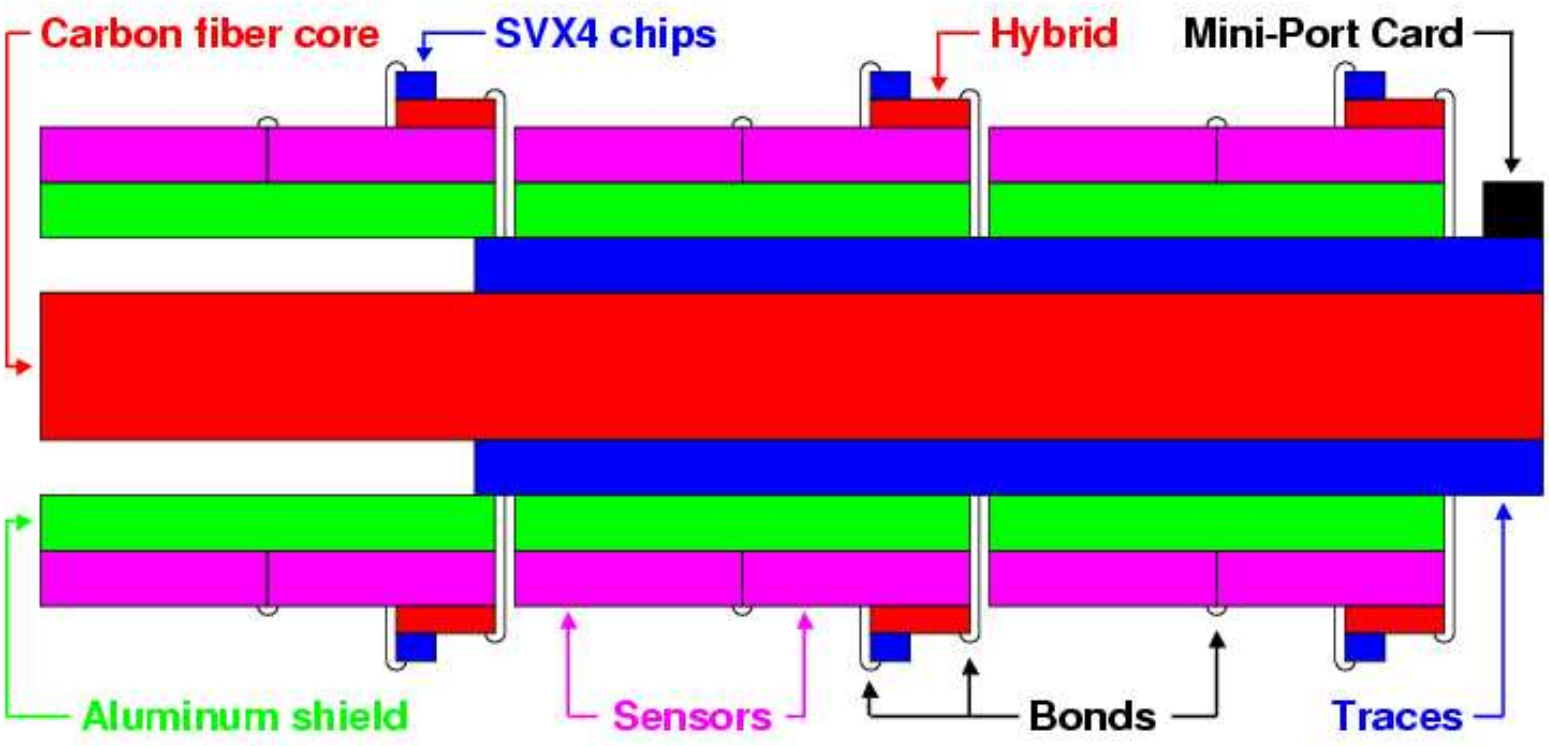


⇐ Run IIa

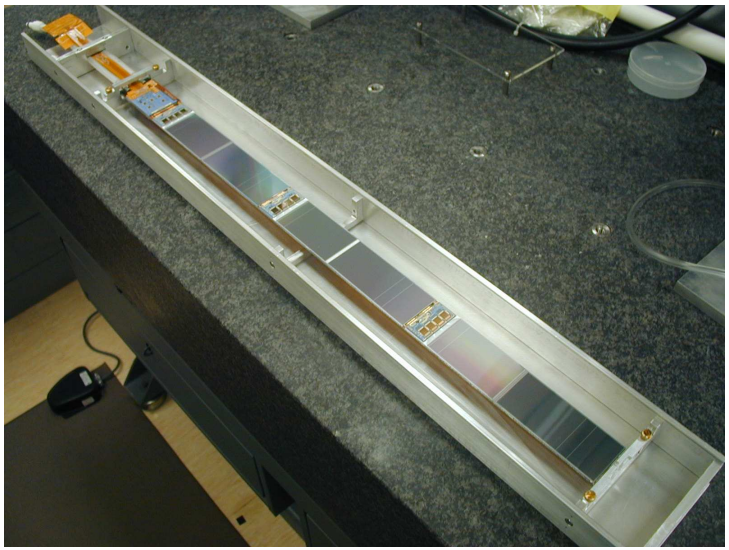
Run IIb ⇒



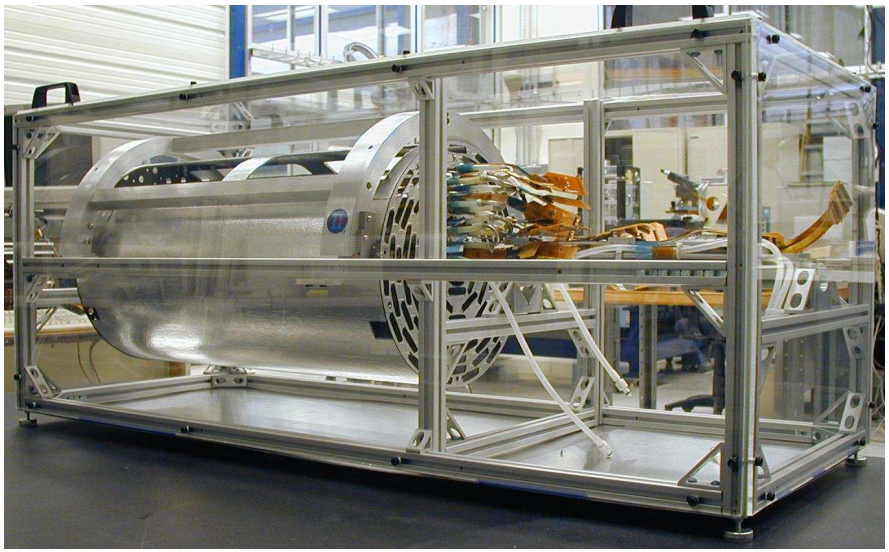
Stave overview



Stave pictures



Prototype stave in testing box



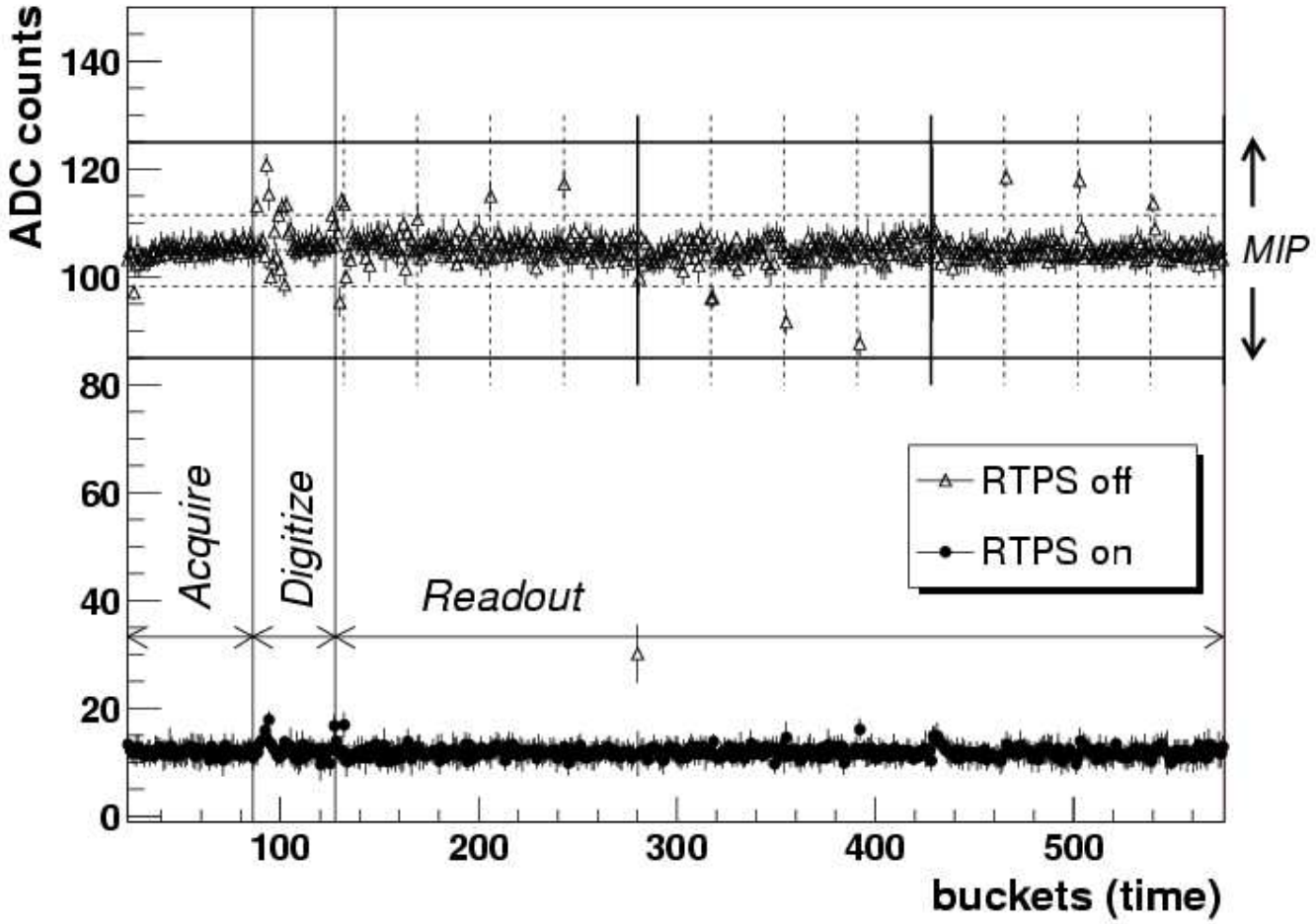
Preproduction staves inserted into barrel

Stave deadtimeless issues

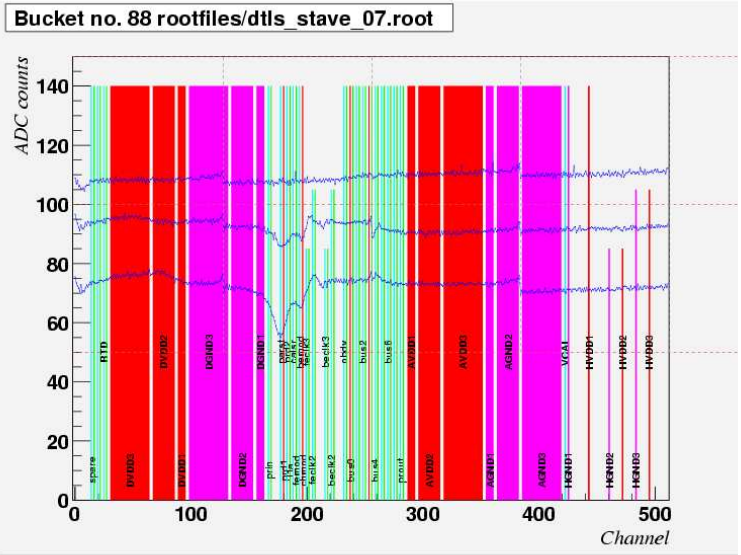
- Deadtimeless operation is challenging: lots of potential sources of pickup (coupling from bus cable into sensors, resistive effects in power traces, inductive coupling between hybrids)
- Optimal configuration combines digital ground for hybrids (less resistance), grounded 50 μm thick shield

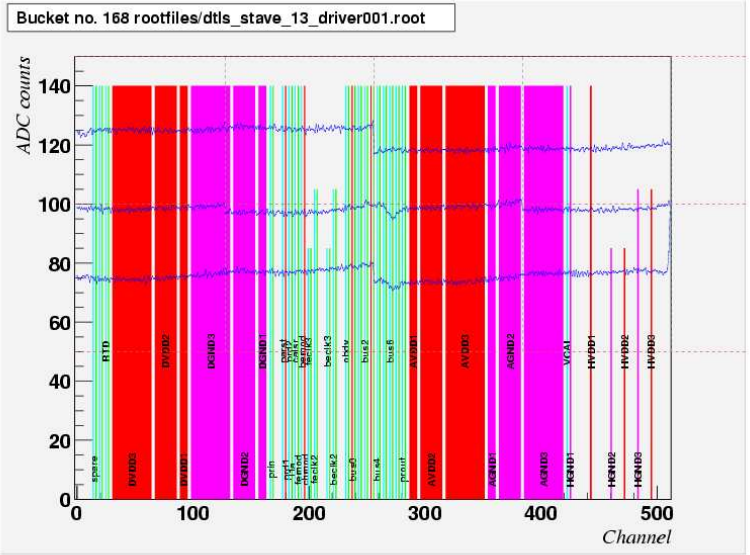
Stave deadtimeless performance

A few pedestal fluctuations during readout, but RTPS eliminates these problems



Pickup from individual traces





First bus cable design exhibited severe pickup from the front-end clock and from other signals used during digitization (also during readout)

Thicker shield, changed trace layout, and decreased currents during readout eliminated most problems and reduced those remaining to a very small level (3-5 counts)

Conclusions

- SVX4 chip was a very successful design (PHENIX, Jefferson Labs, SSRL have expressed interest)
- Demonstrating the success of the stave concept is important for future silicon tracker designs (e.g. upgrades at ATLAS)
- Overall, we are very pleased with the outcome of preproduction (and wish we could have finished the project!)

Backup Slides

Causes of death for SVXII

- Initial luminosity projection of 15 fb^{-1}

Layer	Lifetime (cause of death)
L00	7.4 (V_{dep})
L0	4.3 (S/N)
L1	8.5 (S/N)
L2	16.7 (V_{dep})
L3	23 (S/N)
L4	14 (V_{dep})
Portcards	5.7 (DOIM)

htwish

- htwish is an automated program used to test chips and hybrids
- Produces histograms and quality evaluations
- Tests: configuration shift register, pedestal, gain, pedestal uniformity, gain uniformity, linearity, risetime, sparsification, RTPS, and deadtimeless performance (pedestal and gain stability, with and without charge injection, sparsification, RTPS), etc.

More chip yield information

- 895 SVX4.2B chips delivered
- 500 (55.9%) perfect
- 117 (13.1%) fair (exactly 1 bad capacitor)
- 81 (9.0%) had more than one bad capacitor
- 59 (6.5%) had at least one bad channel
- 25 (2.7%) had other chip-wide problems
- 113 (12.5%) were not completely tested or had inconclusive test data (probably good, but we couldn't be sure)

More hybrid yield information

- 117 hybrids produced, 108 passed initial testing (including 5 successfully repaired)
- 2 failed because of bad cpaacitors
- 1 hybrid was broken during repair
- 1 hybrid had a broken RTD
- 5 hybrids had hybrid-wide problems
- 5 hybrids damaged during encapsulation (and not burned in)
- 2 hybrids kept for further testing
- 101 hybrids successfully burned in

Module and stave production

- 92 modules produced (62 axial, 30 stereo)
- Overall yield: 83%, typically with 1-2 bad channels on a good module
- 11 staves produced (plus one half-stave), one bad chip on one stave, but otherwise good. Typically ~10 bad channels per stave (out of 3072)
- 20 MPCs produced (yield 75%) and 70 bus cables (yield 77%)

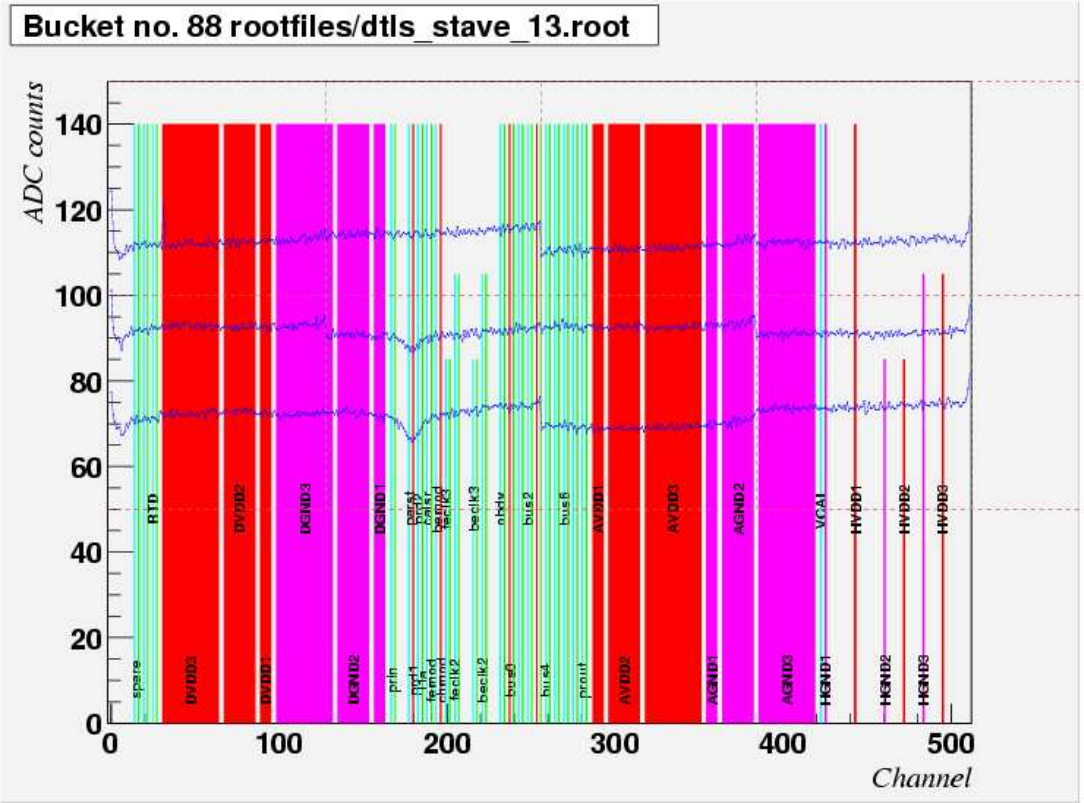
Layer 0

- Due to its extreme closeness to the beampipe, layer 0 requires a separate design
- Narrower sensors, smaller (2-chip) hybrids connected to the sensors by a fine-pitch cable, single-sided only
- Not on the critical path, so given less attention during preproduction
- 16 L0 hybrids produced; 9 worked, and 7 had cable problems (prototype cables were used)
- 5 L0 modules fabricated in total, all good

Radiation lengths

Component	**% X0**	**% total**
sensors	0.676	38.13
structural elements	0.627	35.37
hybrids	0.182	11.78
bus cable	0.021	1.16
Total	**1.774**	**100**

Pickup during digitize



Pickup during readout